

# LS720

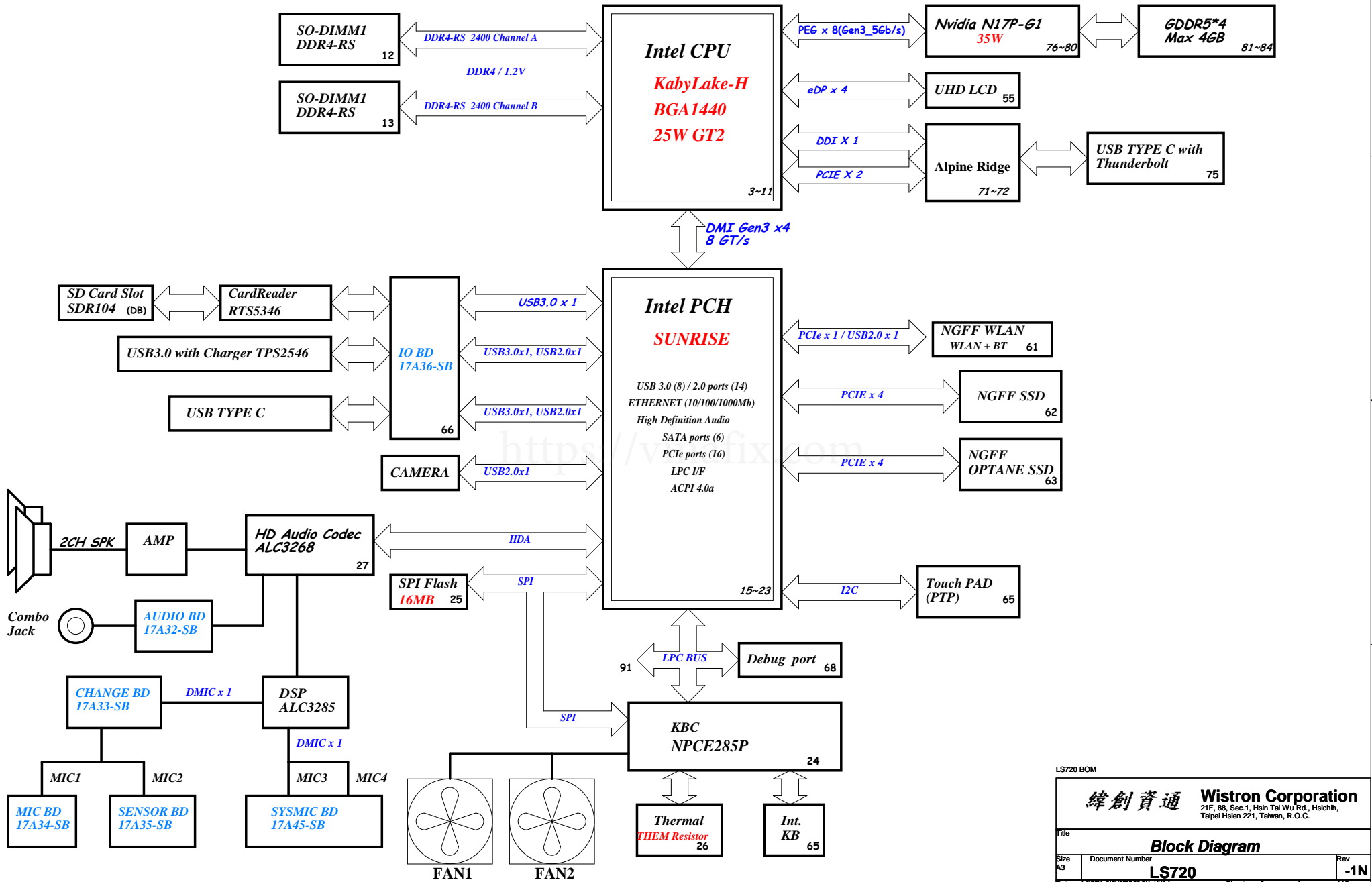
## Schematics Document

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<b>Cover Page</b>					
Size A4	Document Number <b>LS720</b>				Rev <b>-1N</b>
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# LS720 KBL-H Board Block Diagram



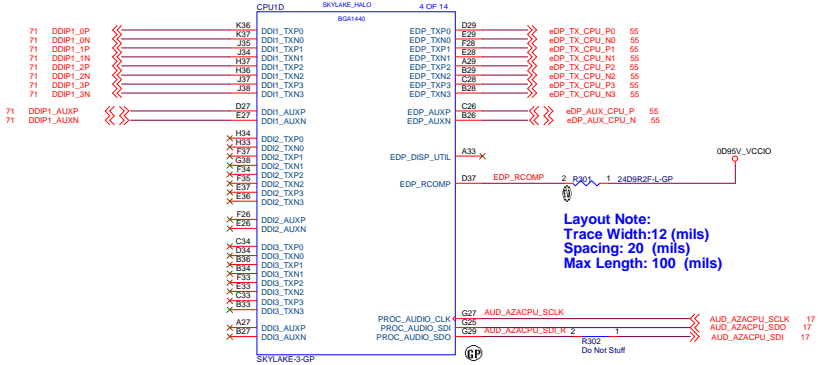
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SSID = CPU



Layout Note:  
Trace Width: 12 (mils)  
Spacing: 15 (mils)  
Max Length: 400 (mils)

Thunderbolt



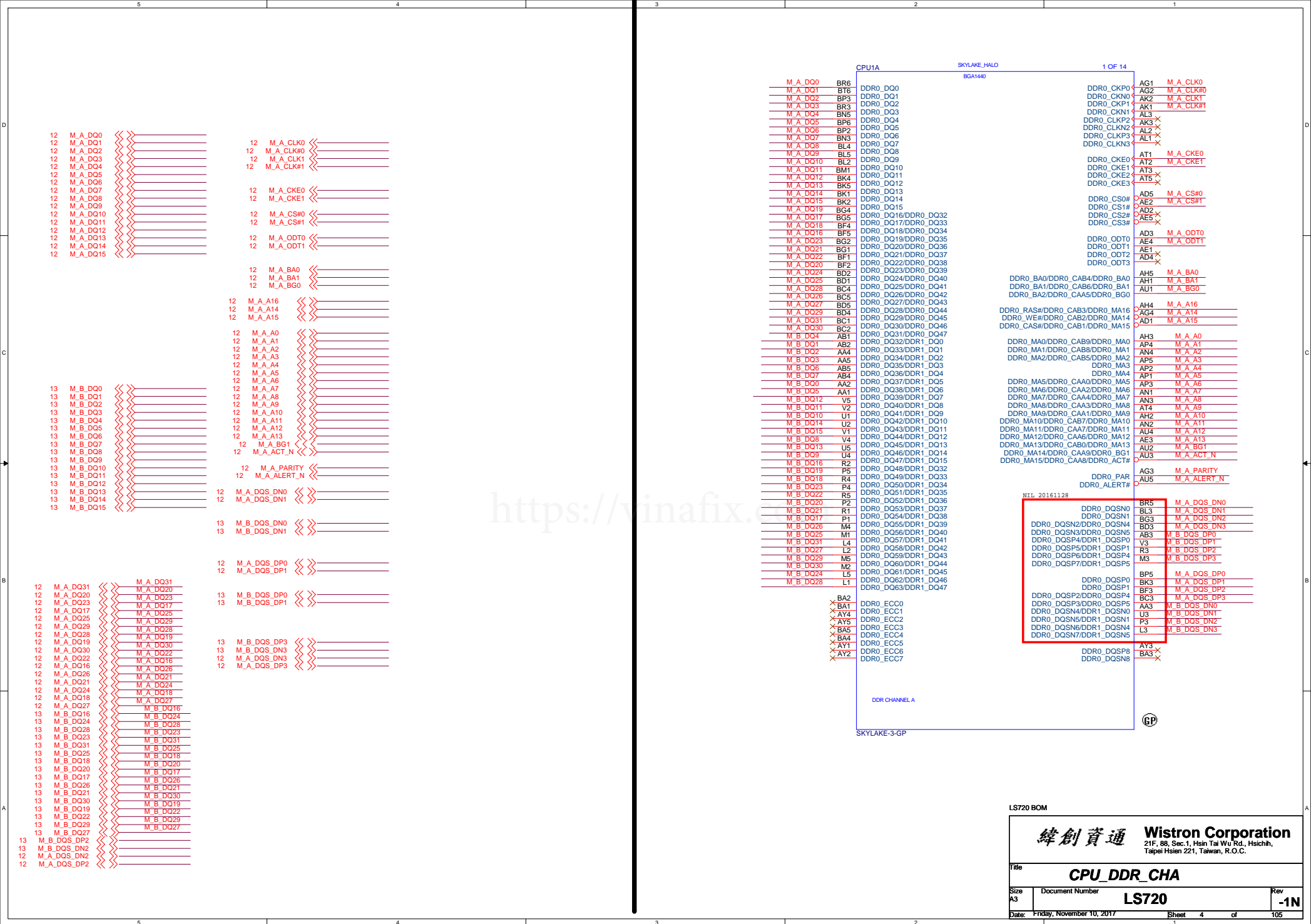
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Spacing: 20 (mils)  
Max Length: 100 (mils)

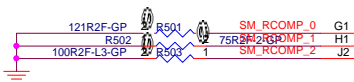
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CPU (PCIe/DMI/FDI)			
LS720		Rev -1N	
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Title			
<b>CPU DDR CHB</b>			
Size A3	Document Number		Rev
	<b>LS720</b>		<b>-1</b>
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**SSID = CPU**

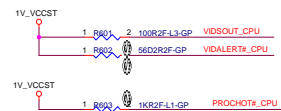
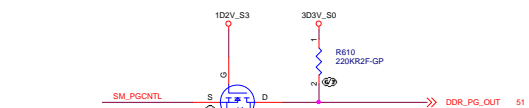
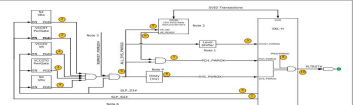
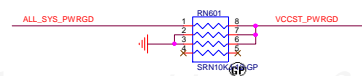
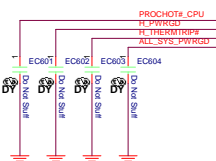
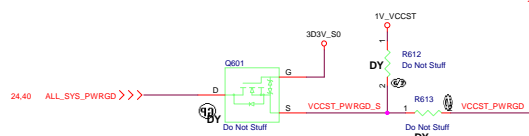


Figure 40-1. SKL H Flow Diagram for SYS\_PWROK/PCH\_PWROK Generation



Change Q602-> VGS(th) max: 1V\_0725  
Do not use 84.00138.F31

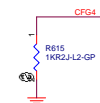


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FPG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

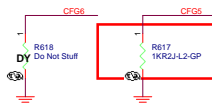


eDF Enable	
CFG4	1:Disable 0:Enable



```
PCIE Port Bifurcation Straps
```

CFG[6:5]	01: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 11: Reserved - Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	---



20150824 install R617

PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.



Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of 1 if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li>• <b>CFG[0]:</b> Shall reset sequence after PCU PLL lock until de-asserted:           <ul style="list-style-type: none"> <li>– 1 = (Default) Normal Operation; No stall.</li> <li>– 0 = Stall.</li> </ul> </li> <li>• <b>CFG[1]:</b> Reserved configuration lane.</li> <li>• <b>CFG[2]:</b> PCI Express® Static 1x6 Lane Numbering Reversal.           <ul style="list-style-type: none"> <li>– 1 = Normal operation</li> <li>– 0 = Lane numbers reversed.</li> </ul> </li> <li>• <b>CFG[3]:</b> Reserved configuration lane.</li> <li>• <b>CFG[4]:</b> eDP enable:           <ul style="list-style-type: none"> <li>– 1 = Disabled.</li> <li>– 0 = Enabled.</li> </ul> </li> <li>• <b>CFG[6:3]:</b> PCI Express® Bifurcation           <ul style="list-style-type: none"> <li>– 00 = 1 x8, 2 x4 PCI Express®</li> <li>– 01 = reserved</li> <li>– 10 = 2 x8 PCI Express®</li> <li>– 11 = 1 x16 PCI Express®</li> </ul> </li> <li>• <b>CFG[7]:</b> PEG Training:           <ul style="list-style-type: none"> <li>– 1 = (default) PEG Train immediately following RESET# de assertion.</li> <li>– 0 = PEG Wait for BIOS for training.</li> </ul> </li> <li>• <b>CFG[18:8]:</b> Reserved configuration lanes.</li> </ul>	I/O	GTL	SE	<p>All processor lines, CFG[2], CFG[6:3] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.</p>

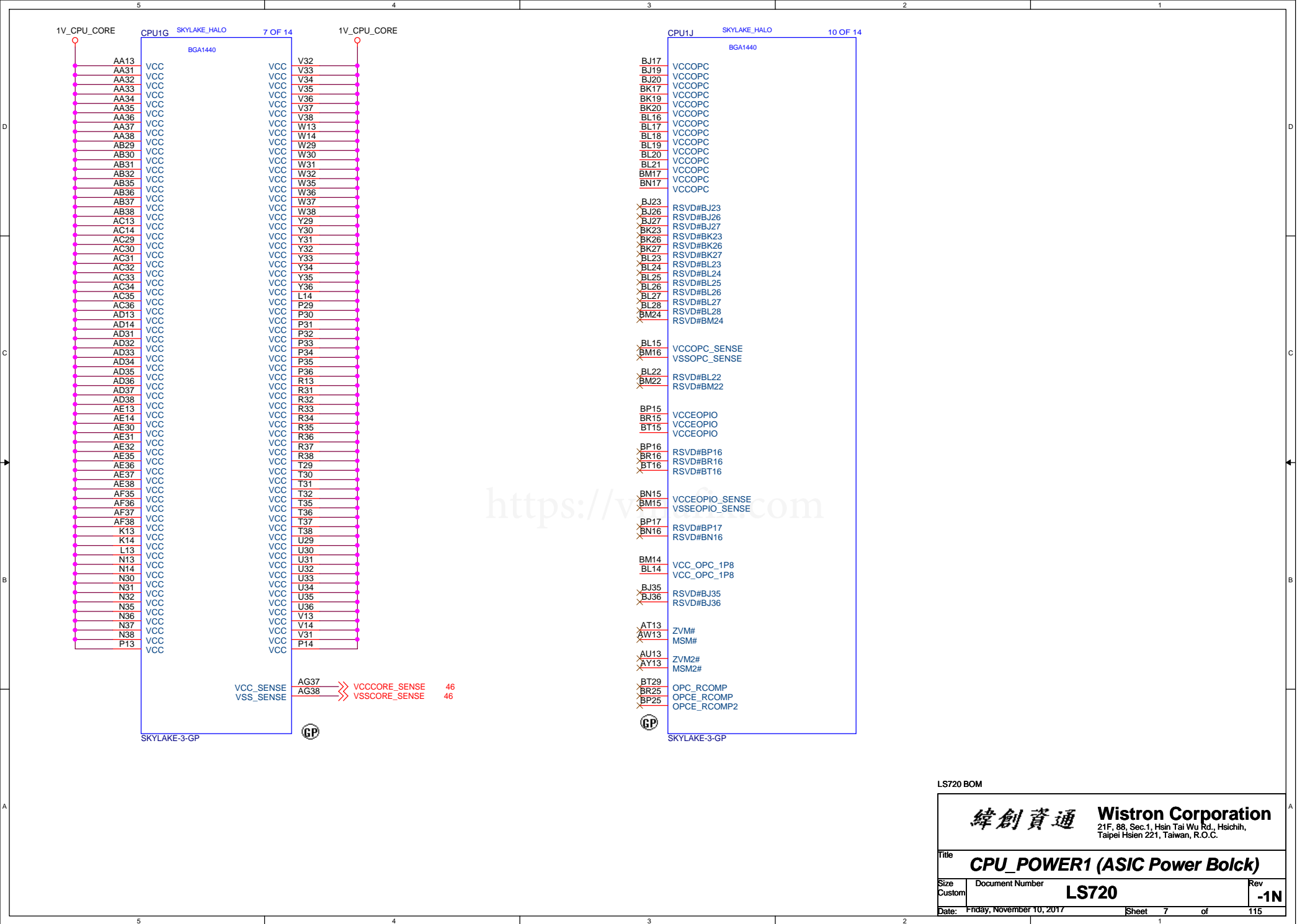
## Processor Internal Pull-Up / Pull-Down Terminations

### Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC <sub>IO</sub>	16-60 Ω
PREQ#	Pull Up	VCC <sub>GT</sub>	3 kΩ
PROC_TDI	Pull Up	VCC <sub>GTG</sub> <sup>1</sup>	3 kΩ
PROC_TMS	Pull Up	VCC <sub>GTG</sub> <sup>1</sup>	3 kΩ
CFG[19:0]	Pull Up	VCC <sub>IO</sub>	3 kΩ

**Note:**

1. For SKL-S it should be  $V_{CCST}$



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TitleCPU\_POWER1 (ASIC Power Bolck)

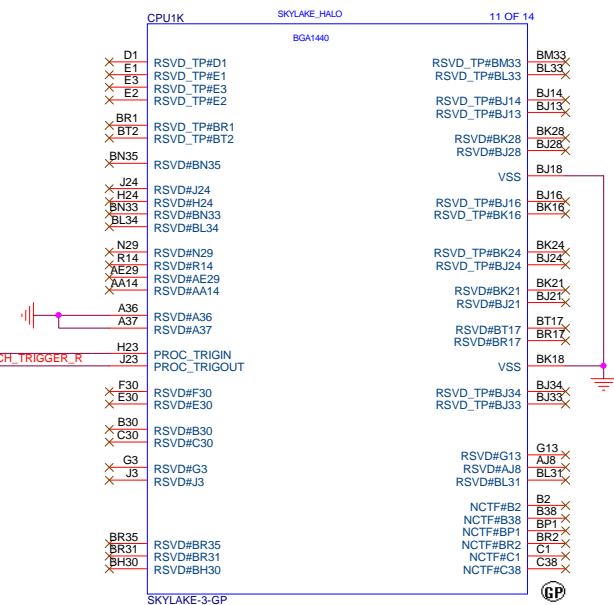
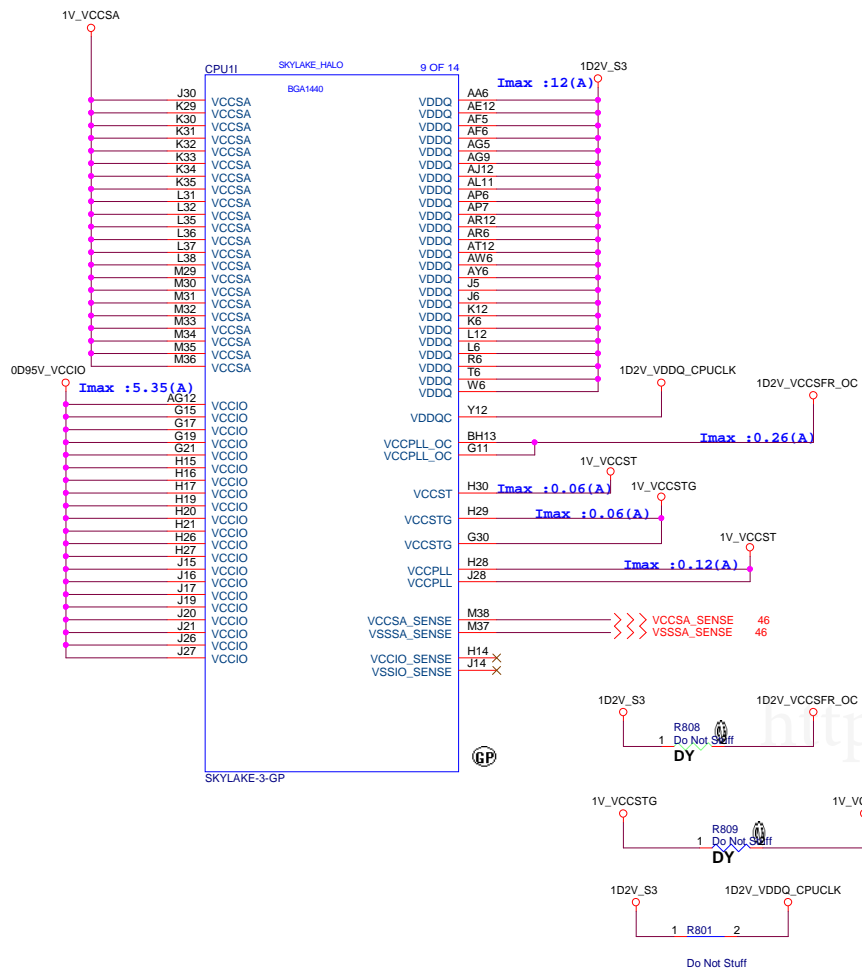
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SSID = CPU

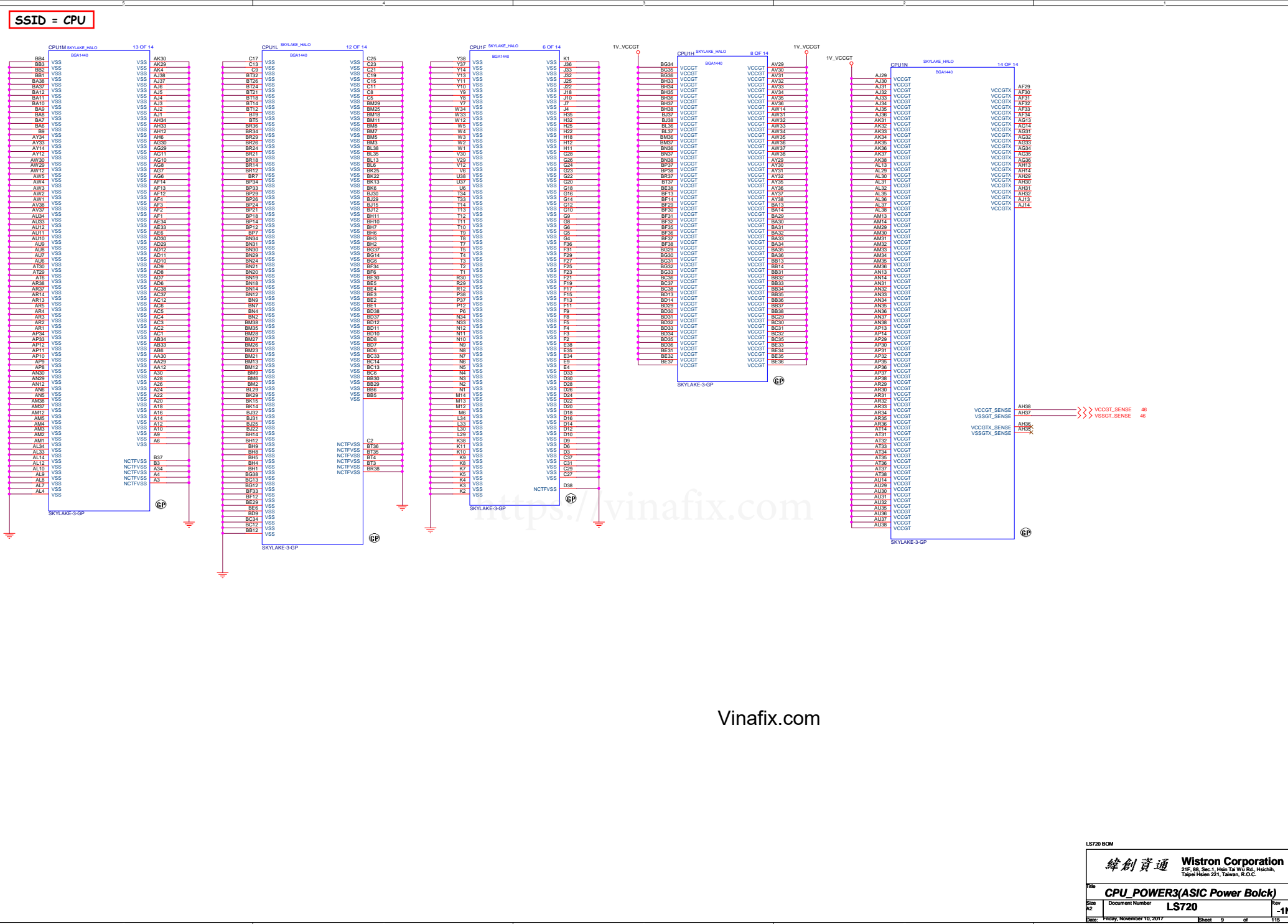


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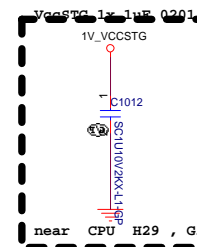
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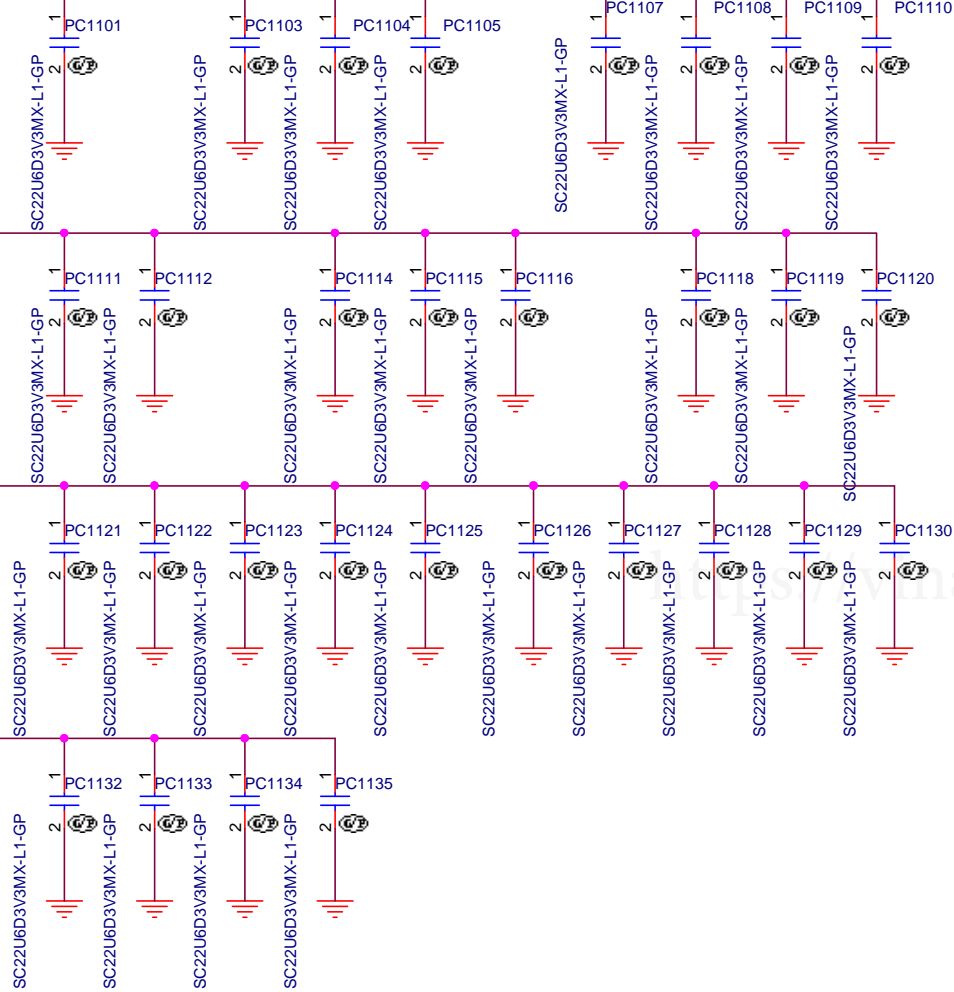


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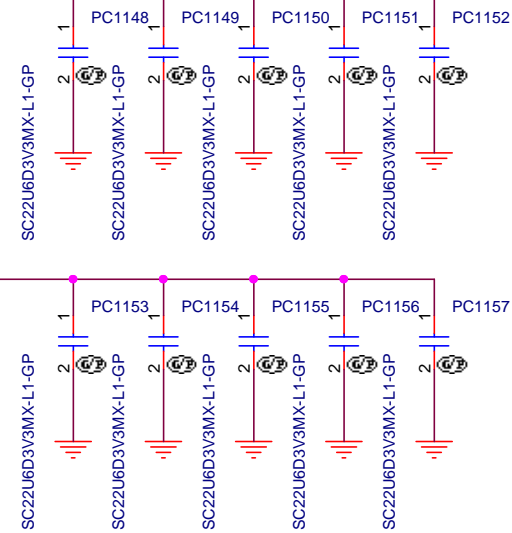


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1V\_VCCGT



1V\_VCCSA



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**CPU (Power CAP2)**Size  
A4

Document Number

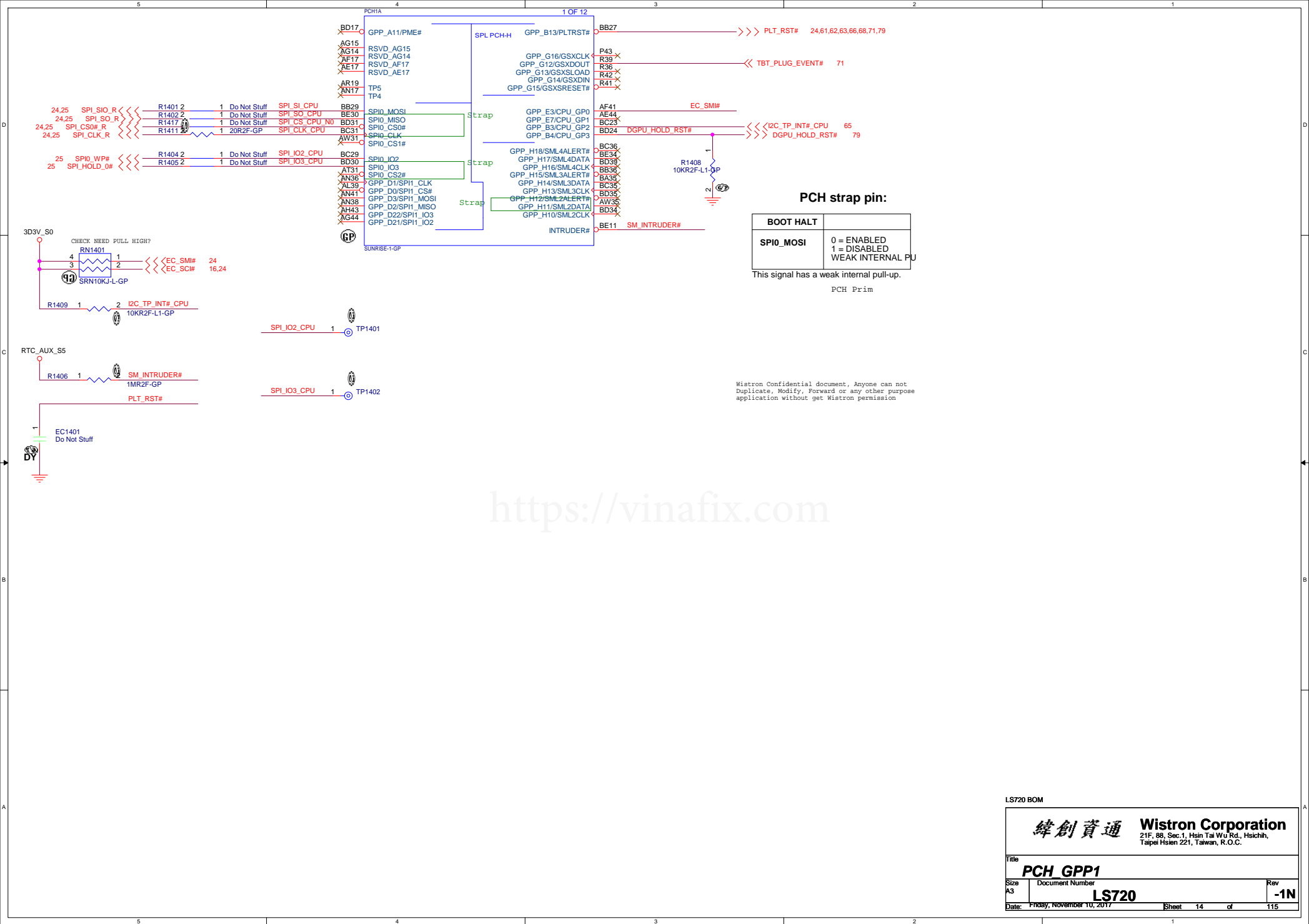
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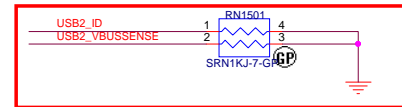
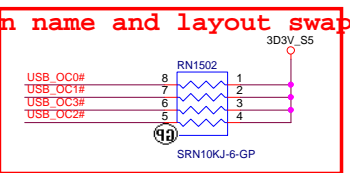
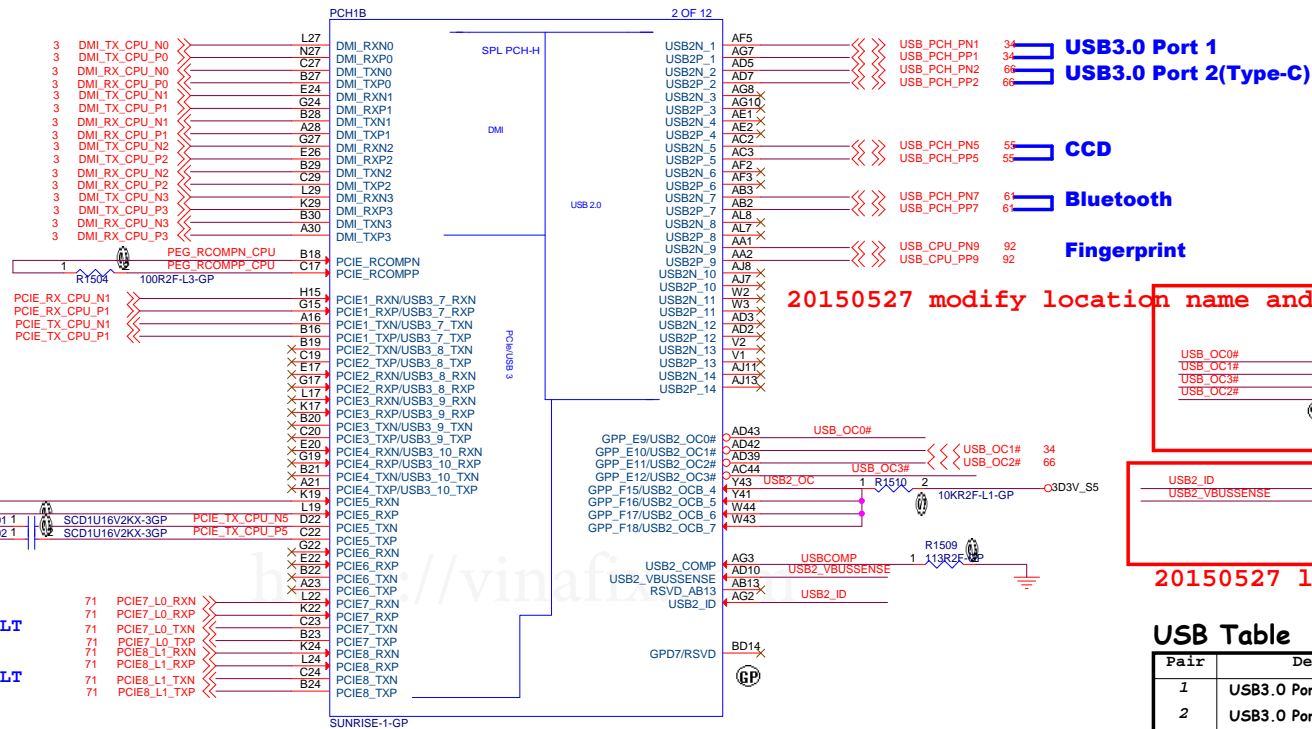




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<b>PCH GPP1</b>			
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**SSID = PCH**



20150527 layout swap

## USB Table

Pair	Device
1	USB3.0 Port 1
2	USB3.0 Port 2(Type-C)
3	
4	
5	CCD
6	
7	Bluetooth
8	
9	Fingerprint
10	
11	
12	
13	
14	

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**PCH PCIE DMI USB**

Size

Document Number

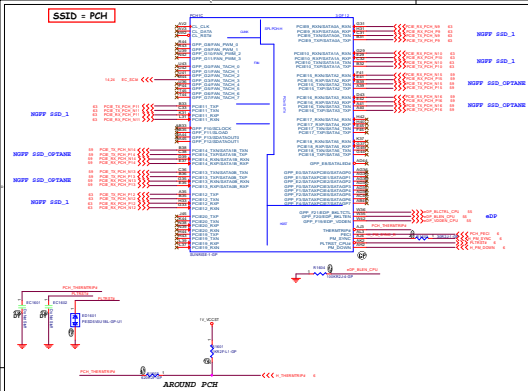
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Rev	-1N
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3 AUD\_AZACPU\_SCLK &lt;&lt;&lt;

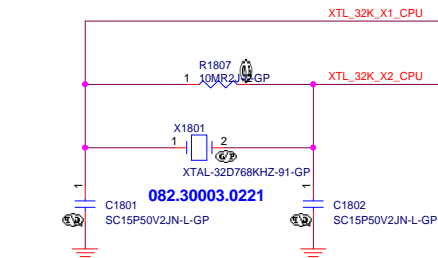
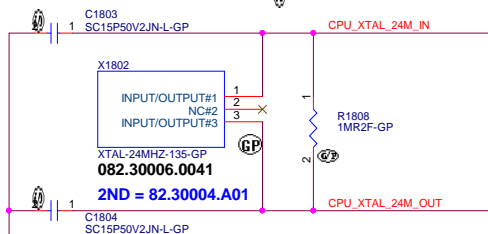
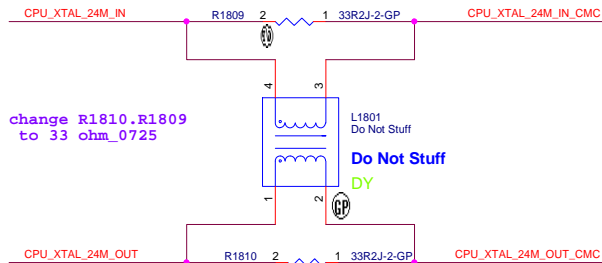
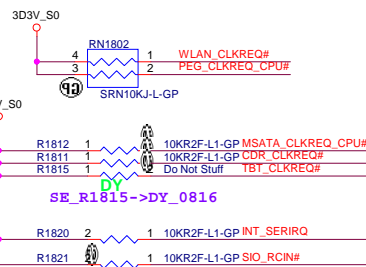
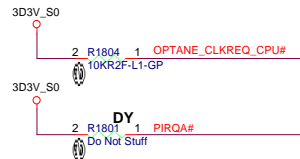


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<b>PCH HDA GPP1 JTAG</b>			
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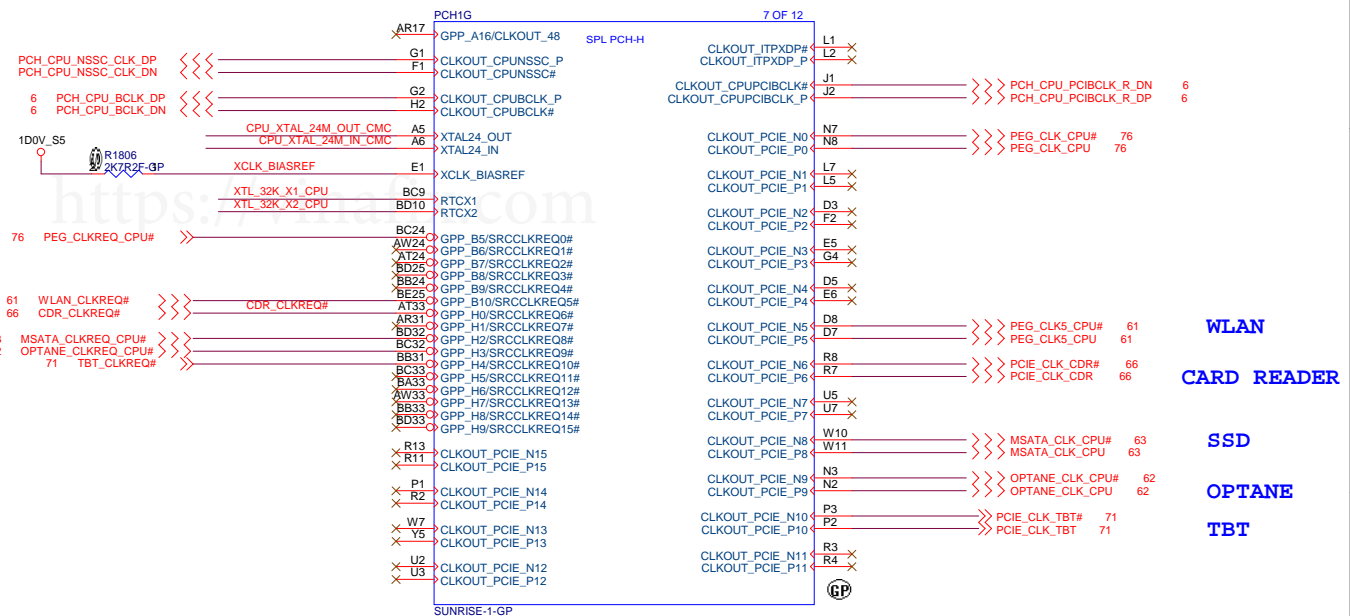
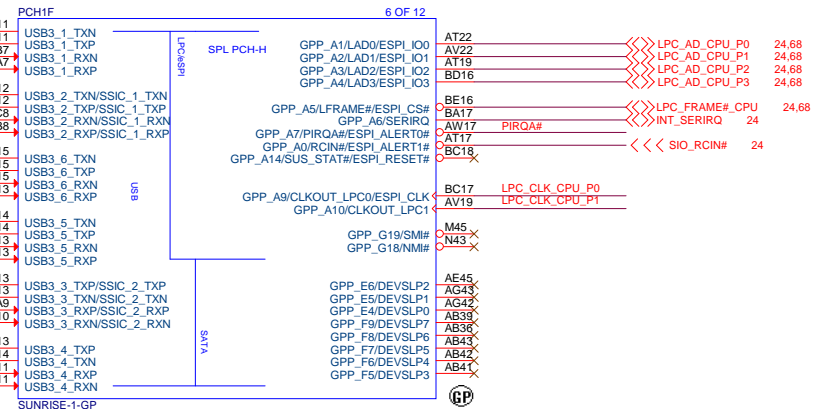
SSID = PCH



20170330  
follow common part rule to use 082.30003.0221

USB3.0 SKT

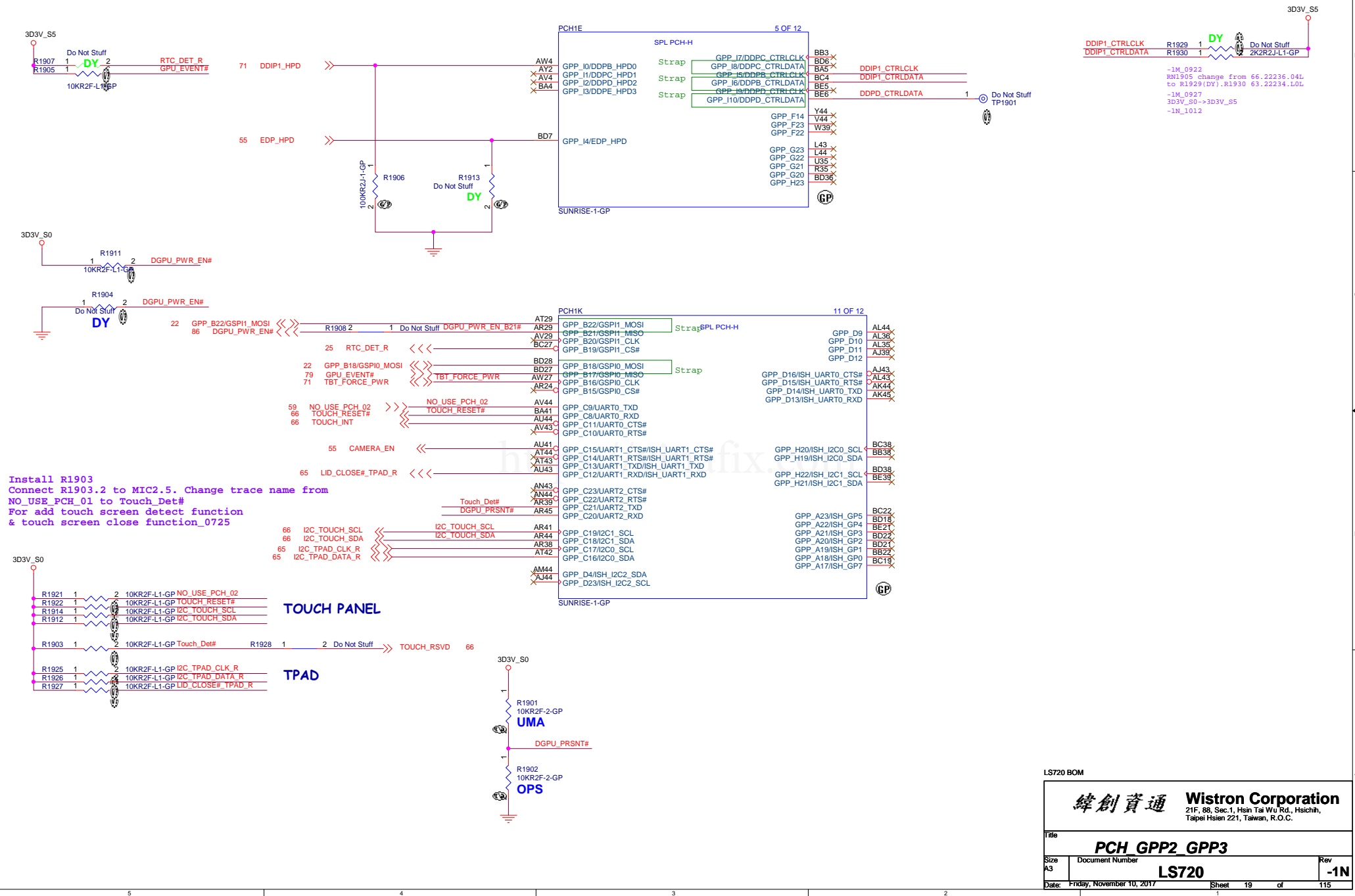
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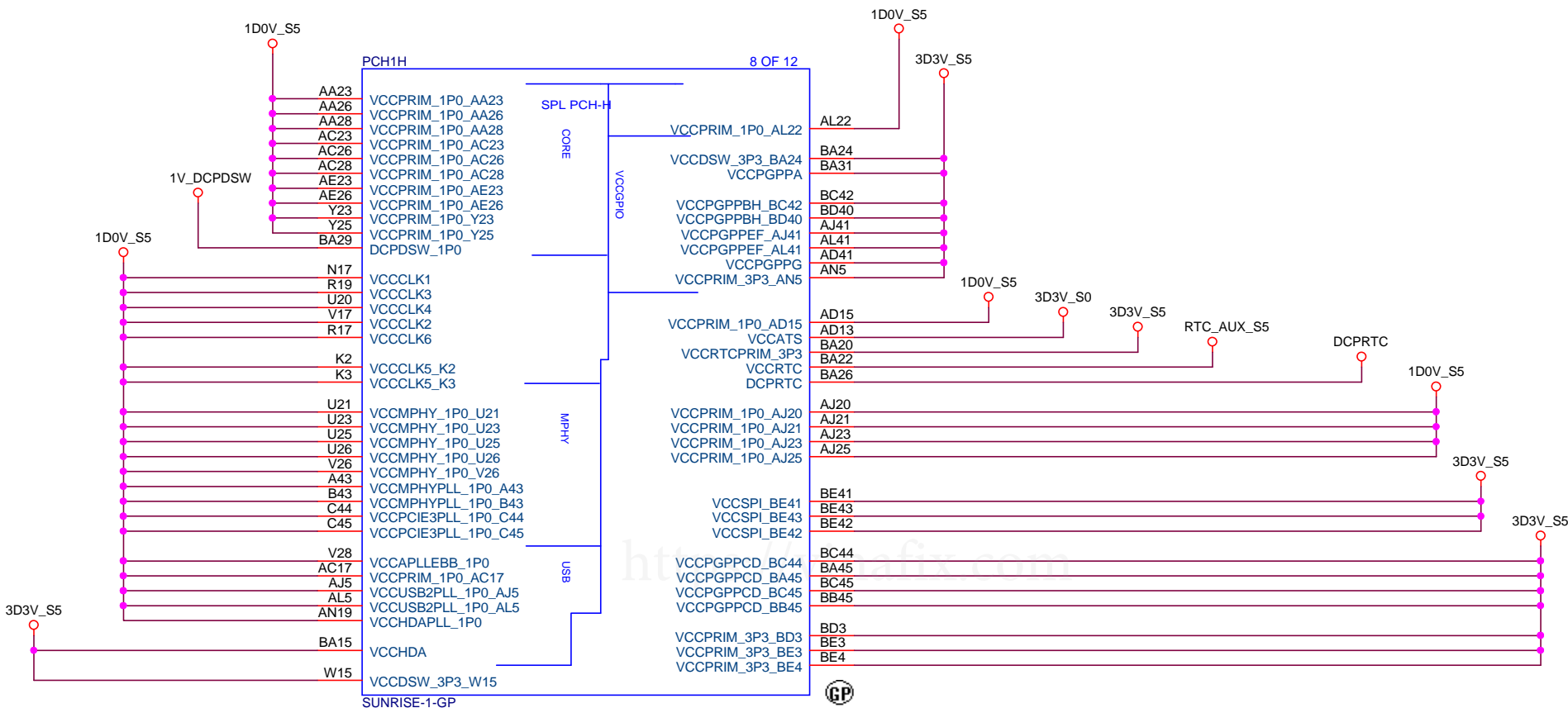
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SSID = PCH



**SSID = PCH**



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**PCH\_POWER\_VCCPRIM\_VCCMPHY**

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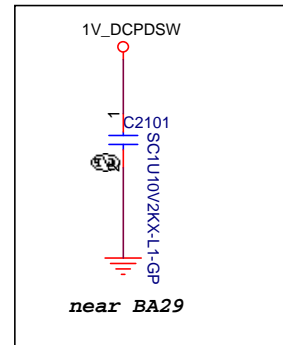
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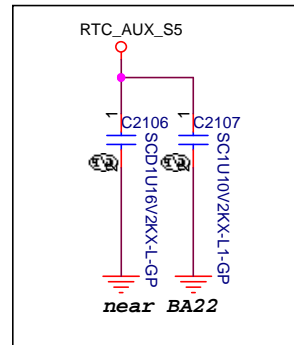
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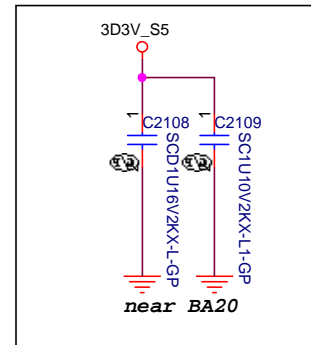
DcpDSW  
1x 1uF



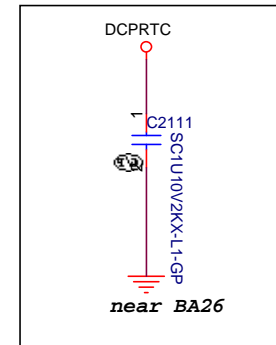
VccRTC  
1x1 uF 1x0.1 uF



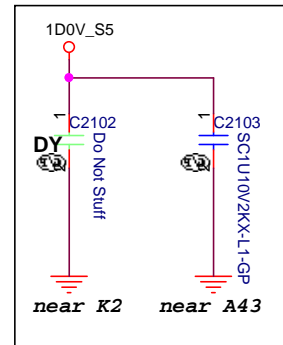
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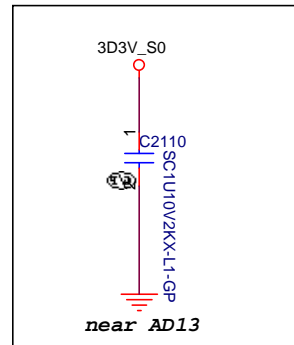
DcpRTC  
1x 0.1uF



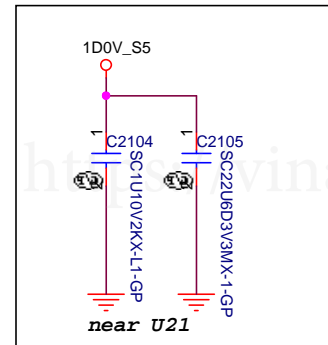
VccMPHYPLL / VccPCIE3PLL  
1x1 uF



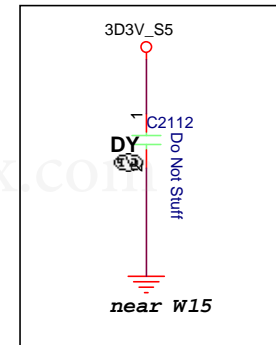
VccATS  
1x1 uF



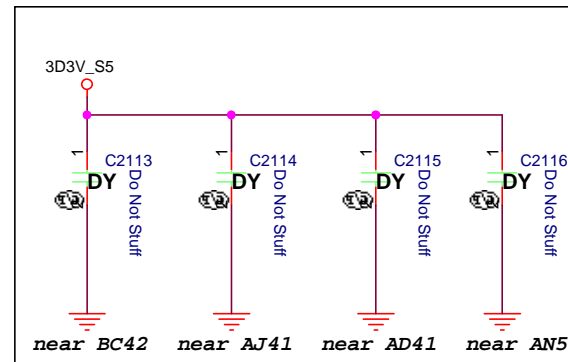
VccMPHY / VccPRIM / VccAPLLEBB  
1x1 uF 1x22 uF



VccDSW  
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG  
/ VccPRIM  
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO)  
(Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/jumper / E/edge)	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V36, AC17, V28	1 uF 22 uF	0402 0805	1 1	E (<3 mm) E (<5 mm)	U21
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	A15, A15, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, V23, Y25	-	-	-	-	-
	V1.0DS W	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AI41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
V1.8A/ V1.8S/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA20
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF 0.1 uF	0402 0402	1 1	E (<5 mm) E (<3 mm)	BA22
	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
V3.3DS W	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

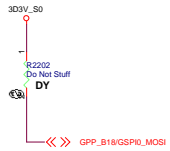
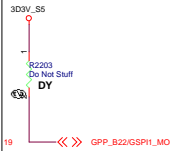
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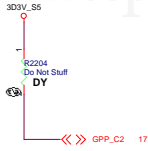
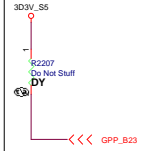
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PCH_POWER_CAP1	
Size A4	Document Number
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Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 R87101						
High	Detected	Detected	Detected	Enable	LPC	Disable	1: SLAVE ATTACHED FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

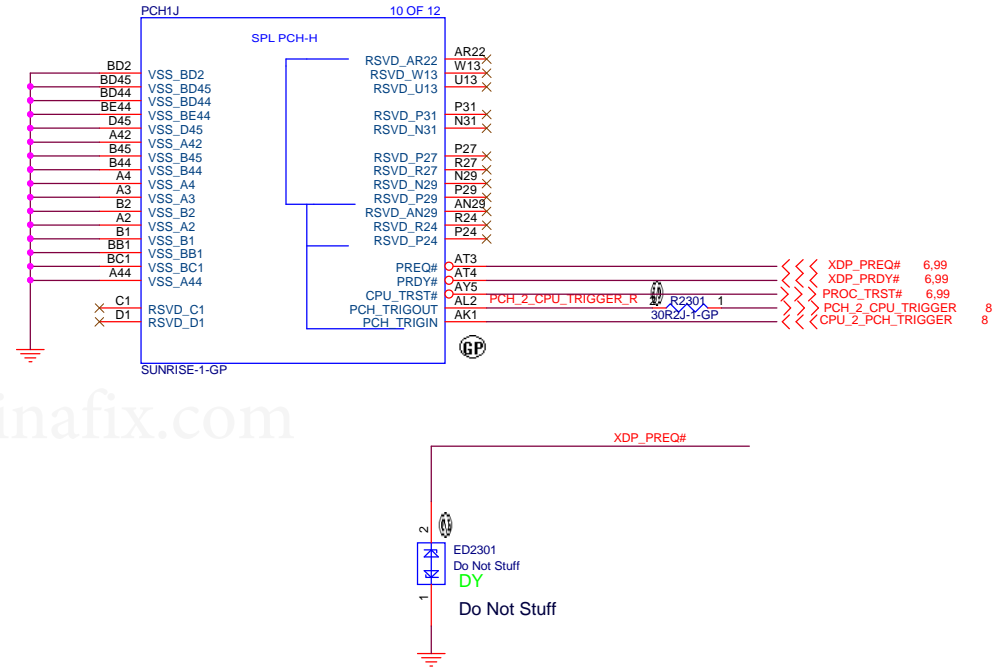
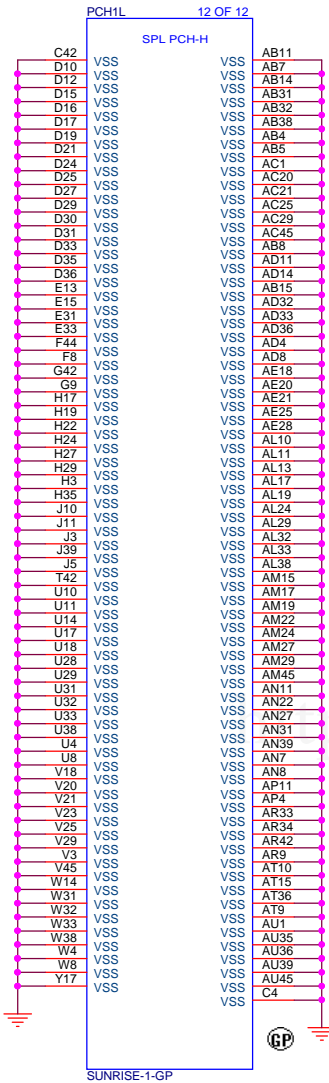
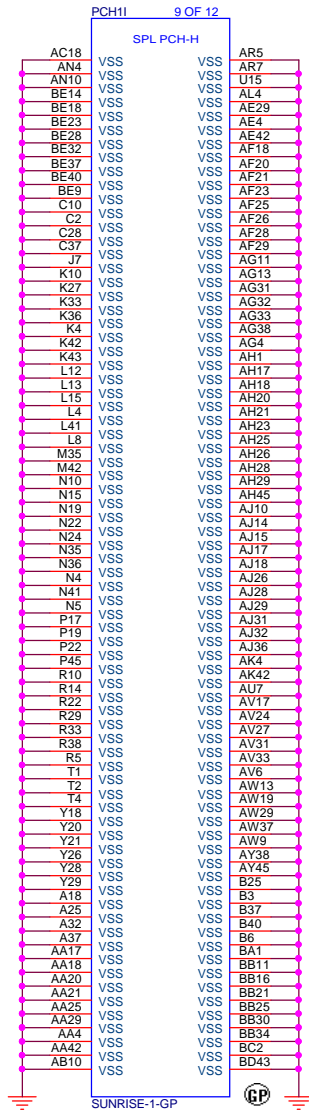
Description	Top Swap Override	eSPI or LPC	TLS Confidentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

[H,S,U,Y] Pull-up Resistors on SPI\_IO2 and SPI\_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the PCH SPI\_IO2 and SPI\_IO3 signals.

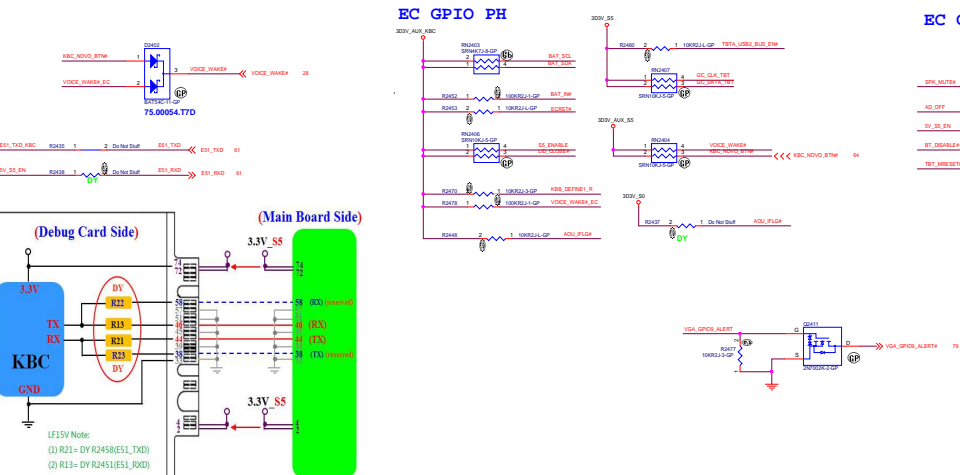
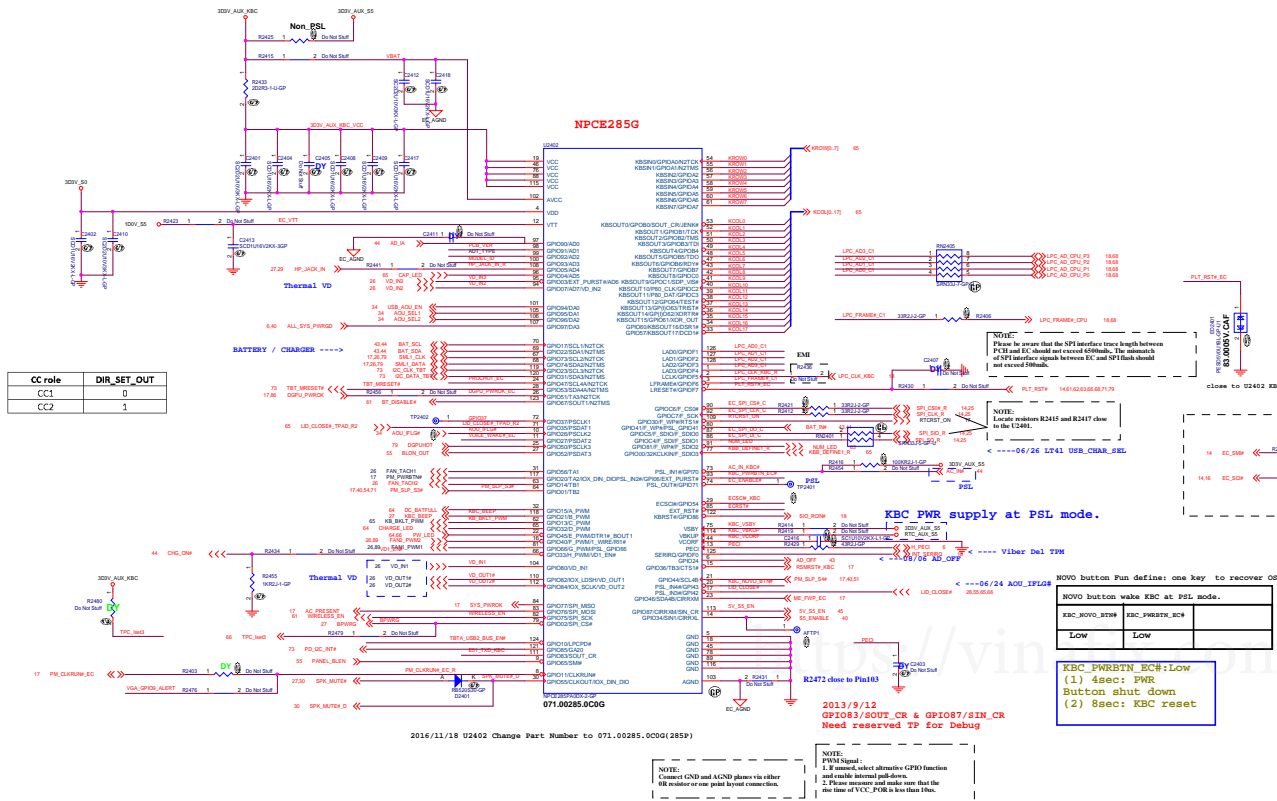
This 1K pull up resistor is no longer needed on Skylake platform and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG.

SSID = PCH



LS720 BOM


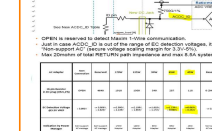
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH_RSVD_VSS	
Size B	Document Number LS720
Date: Friday, November 10, 2017	Sheet 23 of 115
Rev -1N	



PCB VERSION A/D(P/Ns)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
L5720 Inteli Kalydine II	100.0k	10.0k 64.10025A.DL	3.0V
NA	100.0k	20.0k 64.20025A.DL	2.75V
NA	100.0k	33.0k 64.33025A.DL	2.48V
NA	100.0k	47.0k 64.47025A.DL	2.24V
NA	100.0k	64.9k 64.64925A.DL	2.0V
NA	100.0k	76.4k 64.76825A.DL	1.87V
NA	100.0k	215.0k 64.21535A.DL	1.048V

## PCB VERSION

PCB VERSION (APP080)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	1.4V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.8V
SD	100.0K	47.0K	2.24V
SE	100.0K	64.9K	2.8V
-I	100.0K	76.8K	1.87V
-IM	100.0K	100.0K	1.65V
-IN	100.0K	143.0K	1.20V



PIN 3

PIN 1

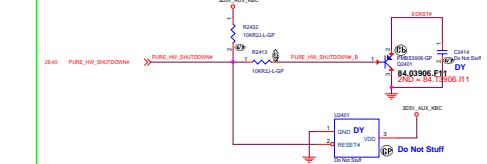
PIN 2

TABLE

	SIGNAL
PIN 1	2B7-vbms(1% TOLERANCE)
PIN 3	---
PIN 2	+

[illegible]

Present: 8304 data long solved.



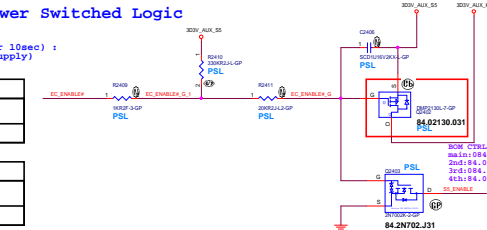
Nuvoton KBC PSL Power Switched Logi

1. Enter PSL mode (Entry S5 after 10sec)  
3D3V\_AUX\_KBC : OFF (KBC PWR supply)

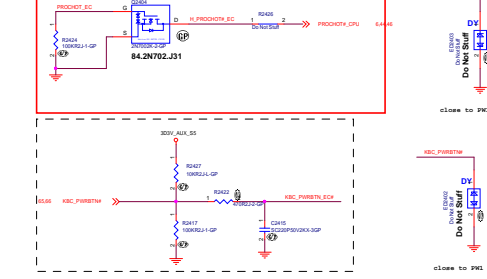
2. At PSL mode (SPEC: S5<10mN)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	SS_ENABLE	3D3V_AUX_KBC
Low	H1	ON



EC: CRI047 IE: 1 A: 1



Nureken KBC PSI Logi

Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

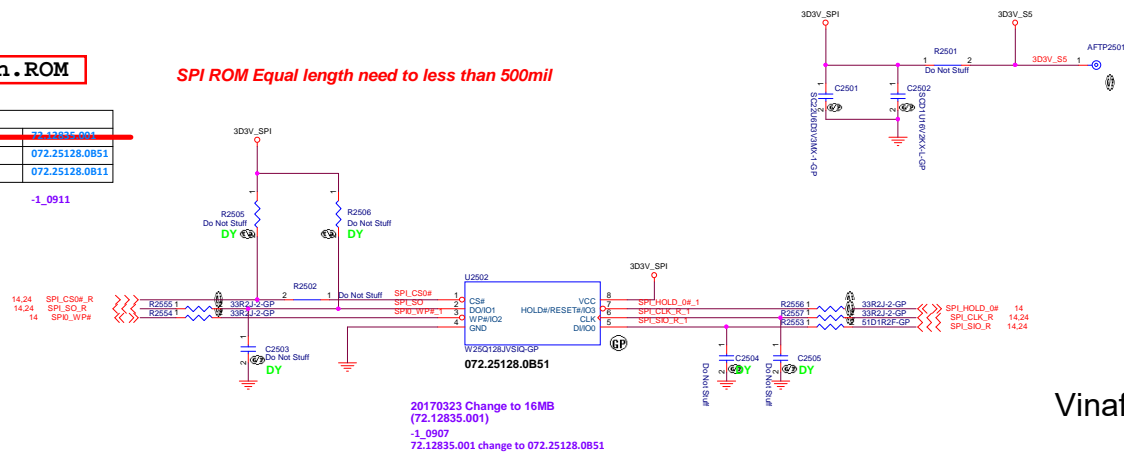


```
SSID = Flash.ROM
```

U2502			
Main	MXIC		72.12835.001
-1 main	WINBOND		072.25128.0B51
-1 2nd	MXIC		072.25128.0B11

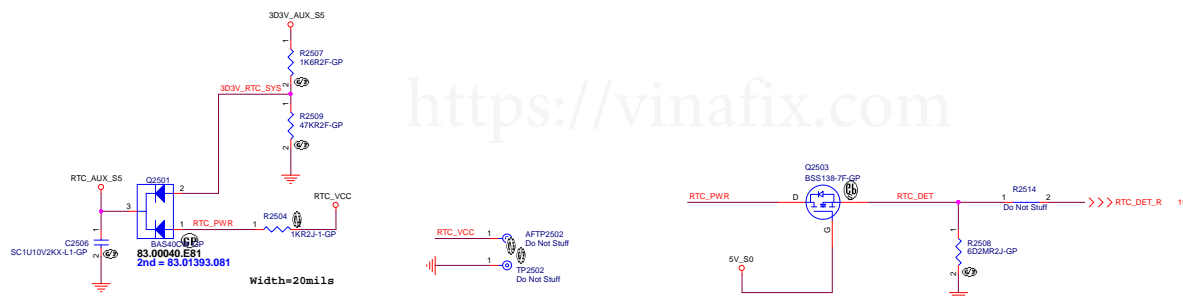
-1\_0911

**SPI ROM Equal length need to less than 500mil**



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SSID = RBATT



LS720 BOM

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>Flash(KBC+PCH)/RTC</b>			
Size A2	Document Number		Rev
	<b>LS720</b>		<b>-1</b>
Date:	Friday, November 10, 2017	Sheet 25 of	115



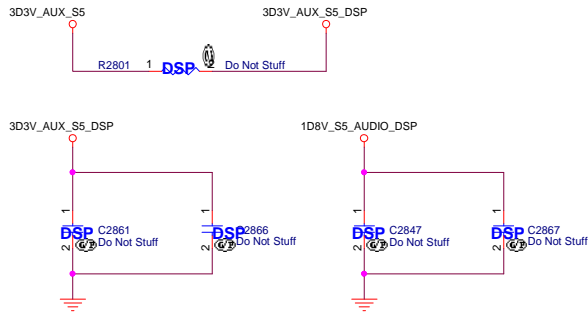


	ENABLE	DISABLE
<b>R808</b>	ASM	NO ASM
<b>R5216</b>	ASM	NO ASM
<b>R4410</b>	ASM	ASM
<b>R4411</b>	ASM	ASM
<b>R4414</b>	ASM	NO ASM

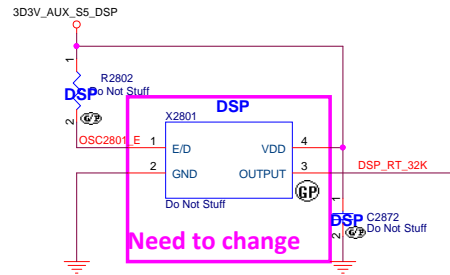
LOGIC

NEED CONFIRM

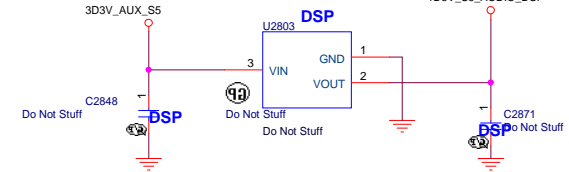
## SD\_DSP->DY\_0804



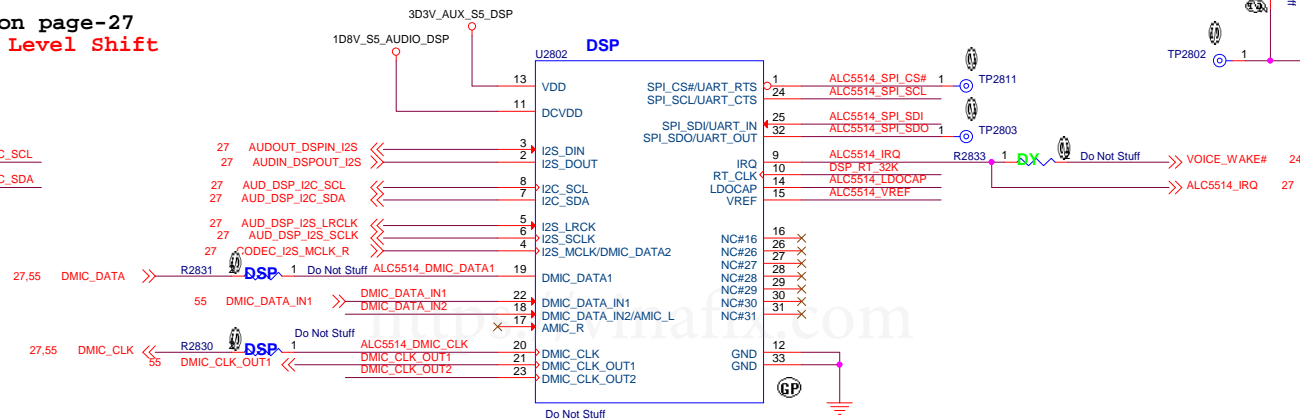
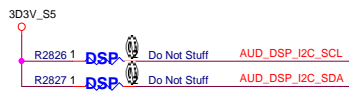
## 32.768KHz OSC circuit



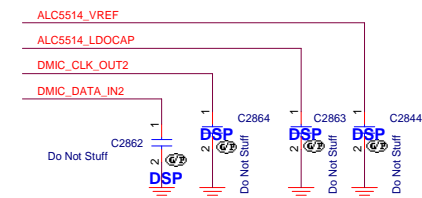
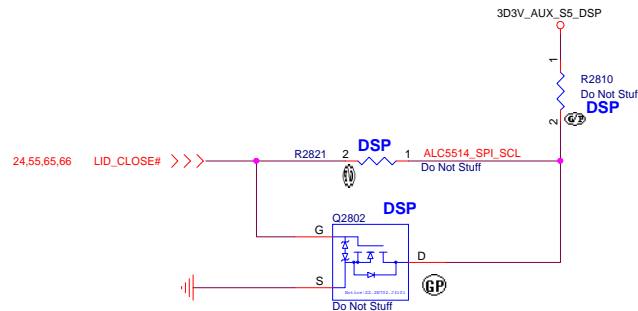
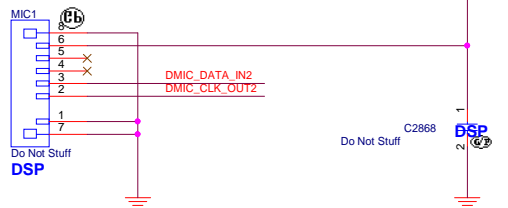
## DSP 1.8V



20170416 pull-up is placed on page-27  
Need check whether need I2C Level Shift

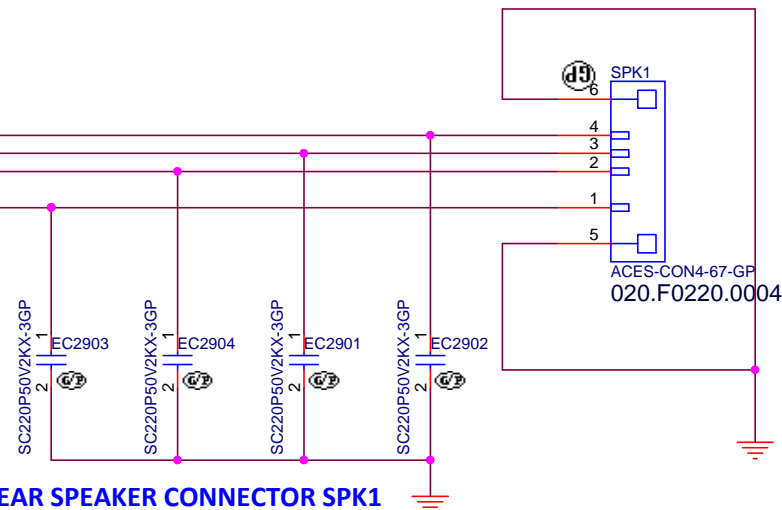


## MB to SYSMIC BD (17A45-SA)



LS720 BOM

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>AUDIO DSP ALC5514</b>		
Size	Document Number	Rev
A3	<b>LS720</b>	<b>-1N</b>
Date:	Friday, November 10, 2017	Sheet 28 of 115

[illegible]

Place these EMI components close to speaker connector.



Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

LS720 BOM

緯創資通

**Wistron Corporation**  
21F, 88, Sec. 1, Hsin-Tai Wu Rd., Hsichih

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO SPEAKER**

Size	A4
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Document Number

## LS720

Rev	-1N
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Date: Friday, November 10, 2017

Sheet 29

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LS720 BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved)		
Size A4	Document Number LS720	Rev -1N
Date: Friday, November 10, 2017	Sheet 31	of 115

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<https://vinafix.com>

LS720 BOM

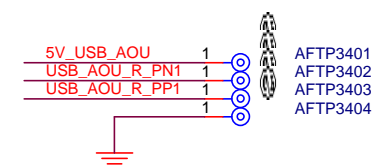
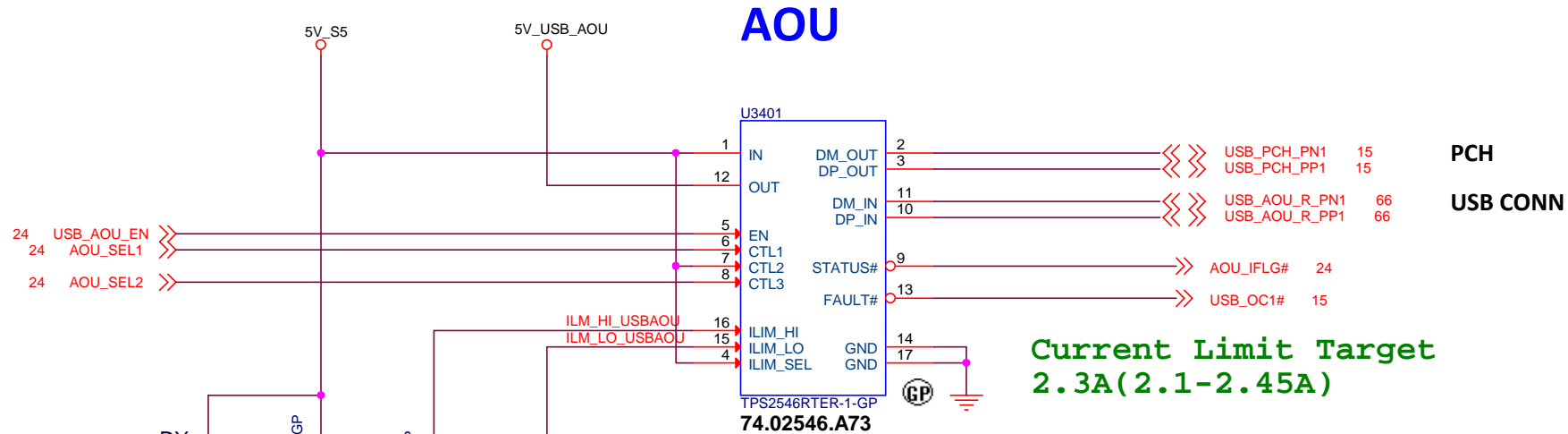
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
RJ45					
Size A4	Document Number LS720				Rev -1N
Date:	Friday, November 10, 2017		Sheet	32	of 115



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<https://vinafix.com>

LS720 BOM

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Card Reader(RESERVED)</b>		
Size A4	Document Number <b>LS720</b>	Rev <b>-1N</b>
Date: Friday, November 10, 2017		Sheet 33 of 115



LS720 BOM

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB Charger</b>			
Size A4	Document Number <b>LS720</b>		Rev <b>-1N</b>
Date:	Friday, November 10, 2017		Sheet 34 of 115

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<https://vinafix.com>

LS720 BOM

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Reserved</b>					
Size A4	Document Number <b>LS720</b>				Rev <b>-1N</b>
Date:	Friday, November 10, 2017			Sheet 35 of	115

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LS720 BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title (Reserved)		
Size A4	Document Number LS720	Rev -1N
Date: Friday, November 10, 2017		Sheet 36 of 115

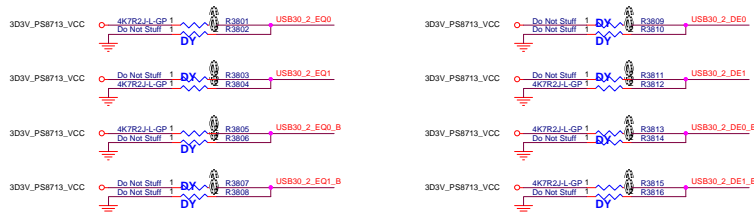
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<https://vinafix.com>

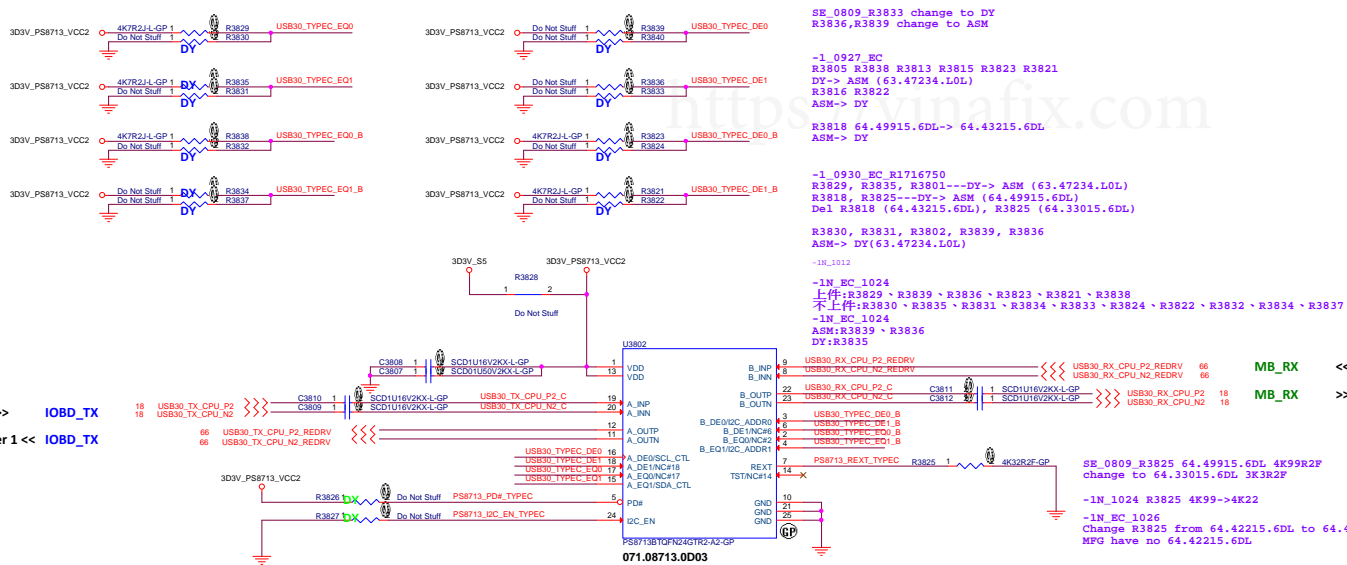
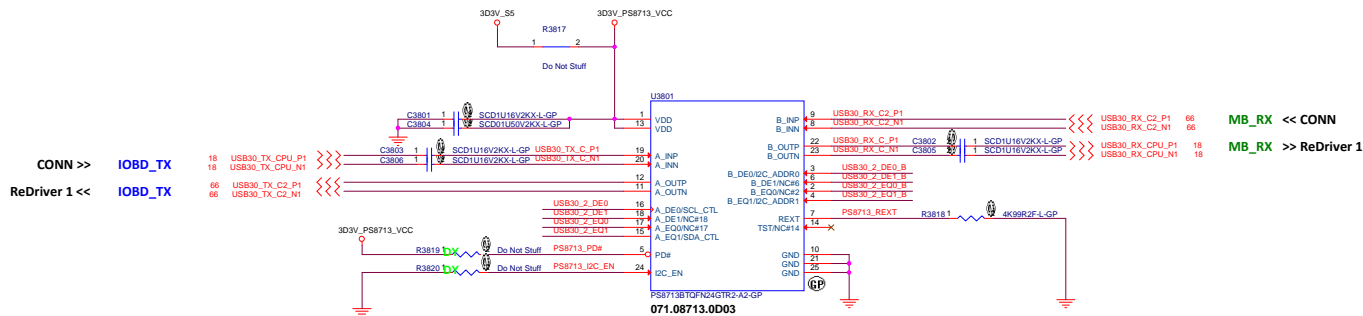
LS720 BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title (RESERVED)		
Size A4	Document Number LS720	Rev -1N
Date: Friday, November 10, 2017		Sheet 37 of 115

## Main Func = USB3.0 Re-driver



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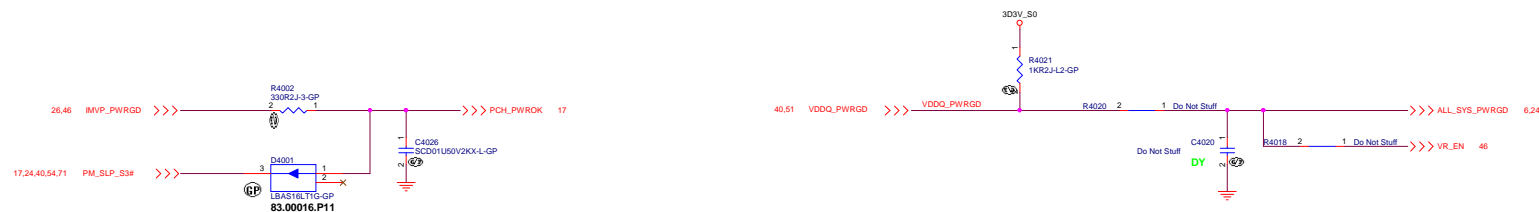
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<https://vinafix.com>

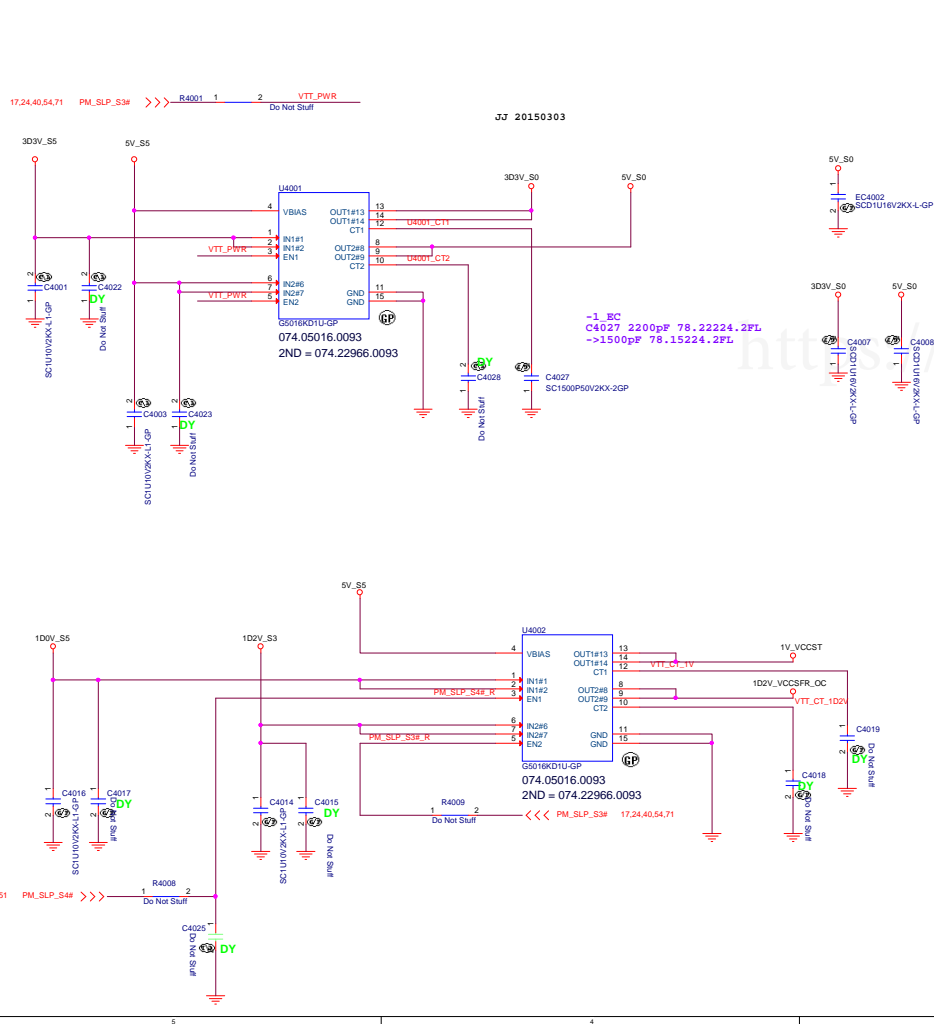
LS720 BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved)		
Size A4	Document Number LS720	Rev -1N
Date: Friday, November 10, 2017	Sheet 39	of 115

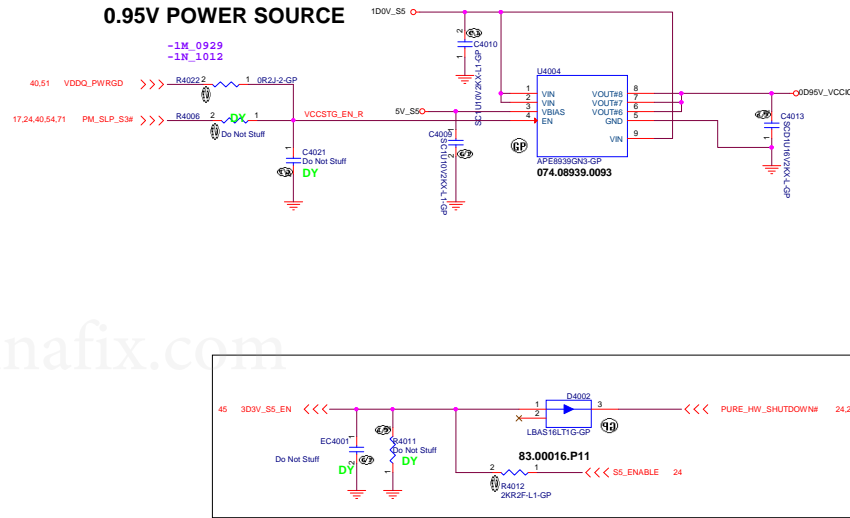
### Power Sequence



## ***ANNIE Run Power***



## 0.95V POWER SOURCE





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LS720 BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved)		
Size A4	Document Number LS720	Rev -1N
Date: Friday, November 10, 2017	Sheet 41	of 115

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LS720 BOM

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved)		
Size	Document Number	Rev
A4	LS720	-1N
Date:	Friday, November 10, 2017	Sheet 42 of 115

**Main Func = BATT CONN**

[illegible]

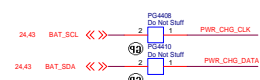
BAT_RST_IN#	PQ501
0 => NO BAT PWR	OFF
1 => BAT PWR ACT	ON

BAT_RELEASE#	PQ501
--------------	-------

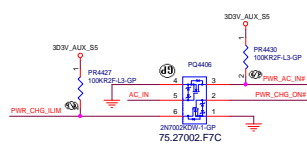
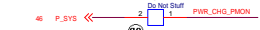
 <b>緯創資通</b>		<b>Wistron Corporation</b> A-21F, 8F, Sec. 1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 224, Taiwan, R.O.C.	
Title	1. NO BATT PWR		OFF
Size A3 Document Number		<b>DC IN/BATT CONN</b>	
<b>LS720</b>		Rev <b>-1N</b>	
Date:	Friday, November 10, 2017	Sheet 43 of	115

## OFFPAGE

SSID = Charger

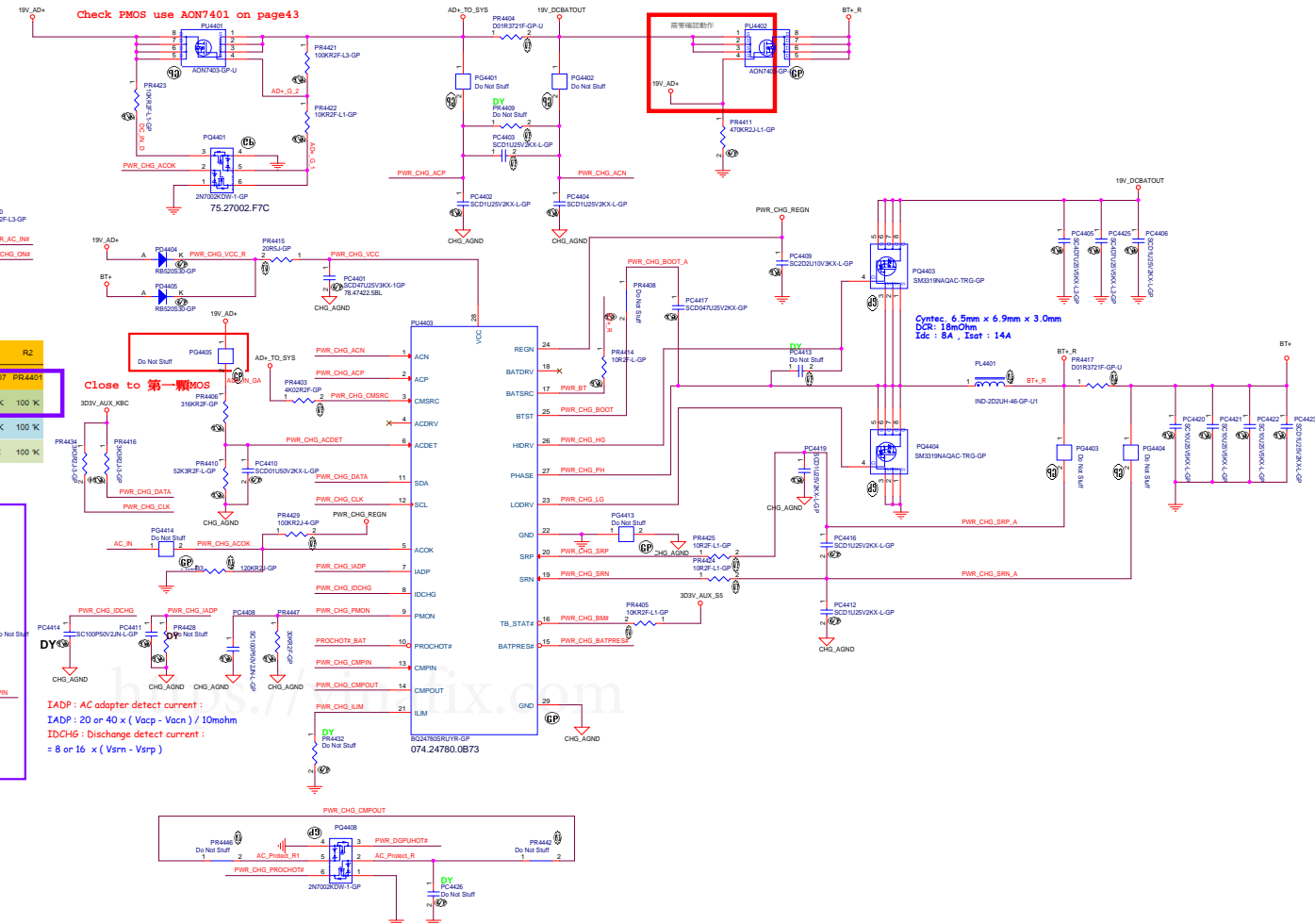
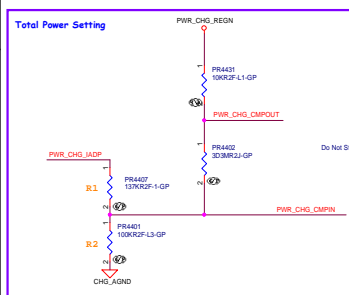


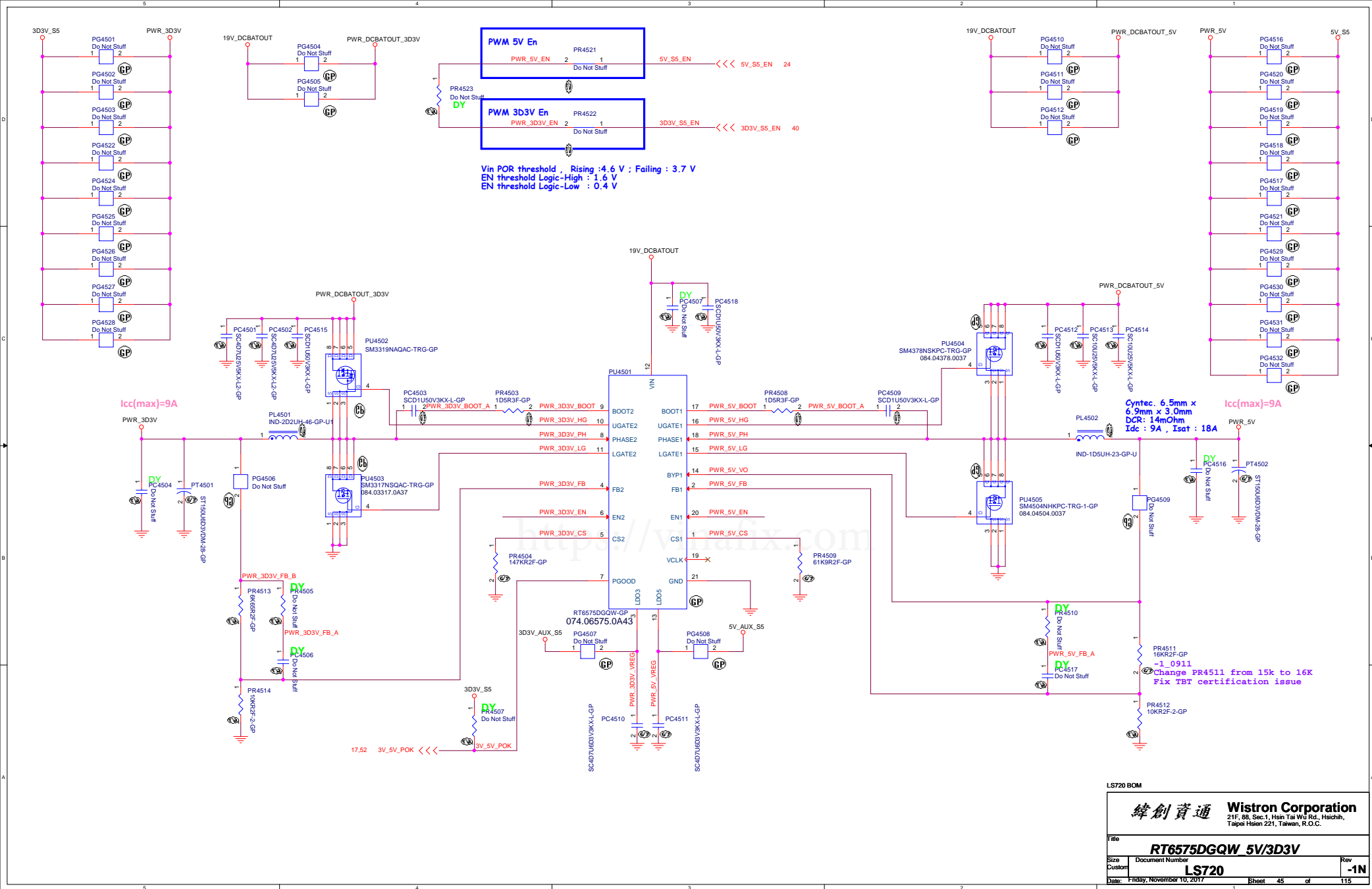
PMON : Total system power



teknisi indonesia

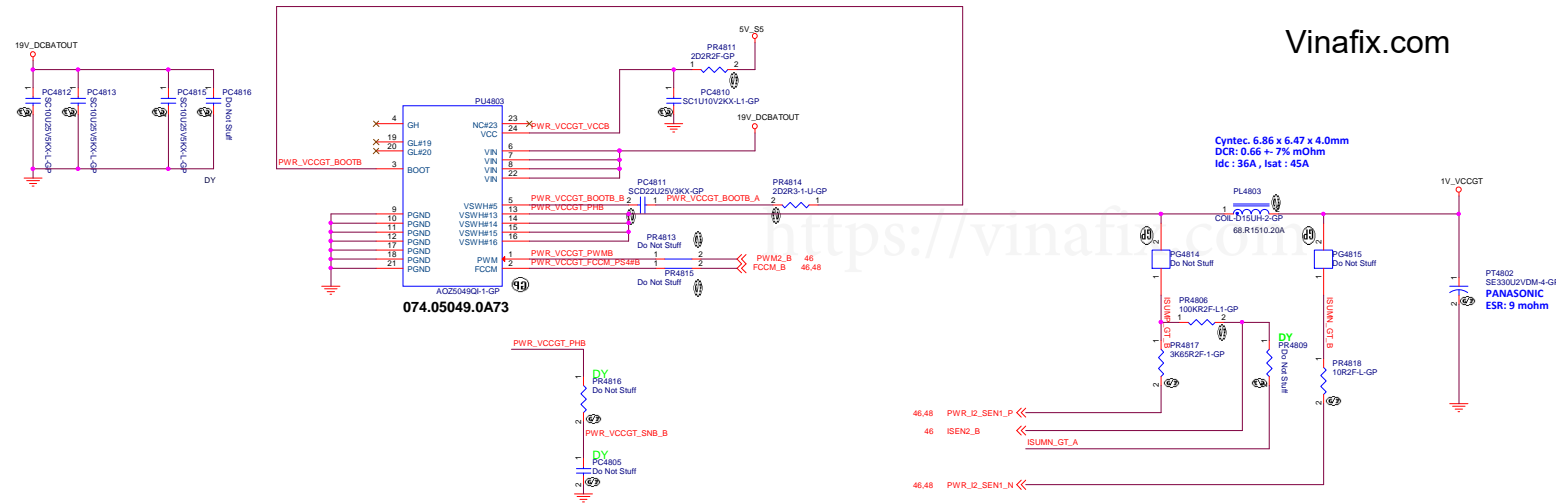
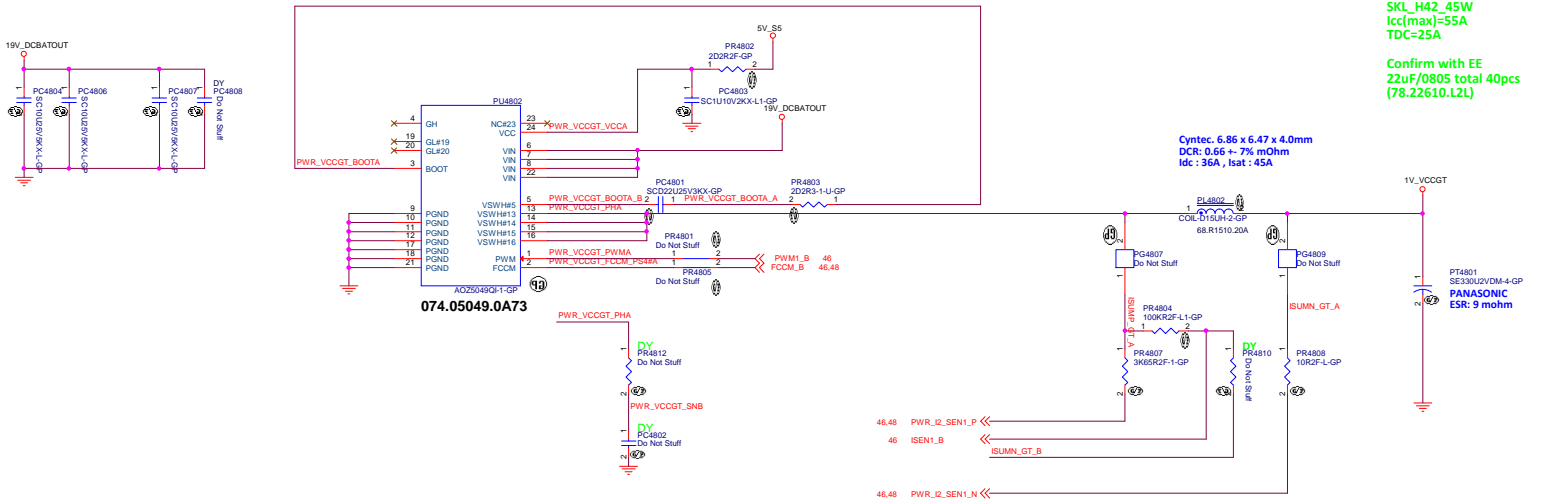
Adaptor			Protect	Sense	Amplifier		R1	R2
Watt	Current	Percent	Current	Resistor	Ratio	IADP	PR4407	PR4401
136.00 W	6.92 A	102%	7.06 A	10 m Ohm	40	2.82 V	137 °K	100 °K











LS720 BOM



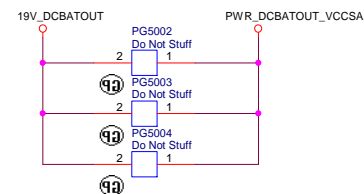
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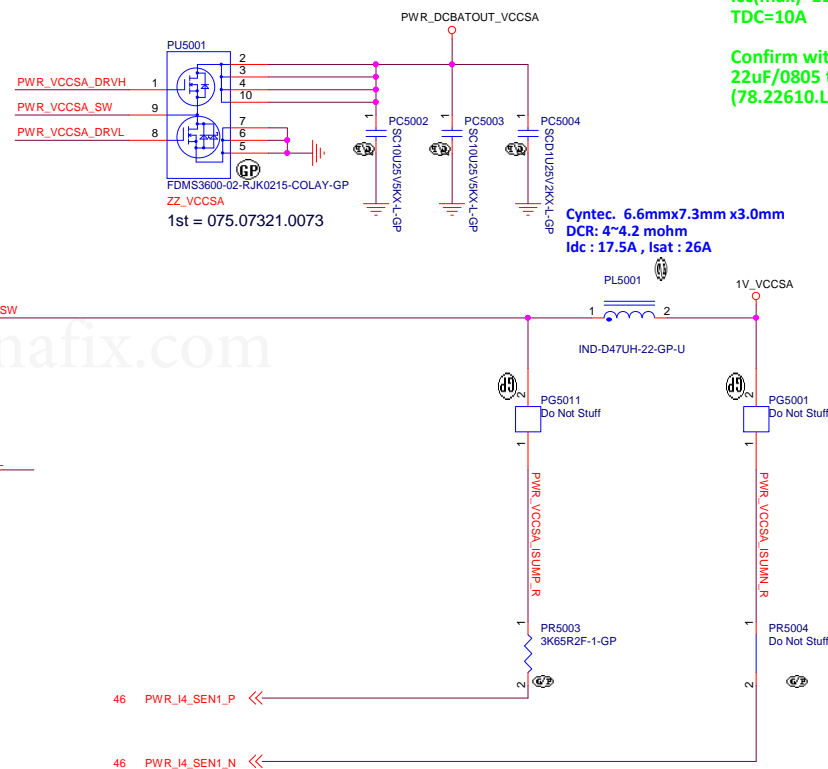
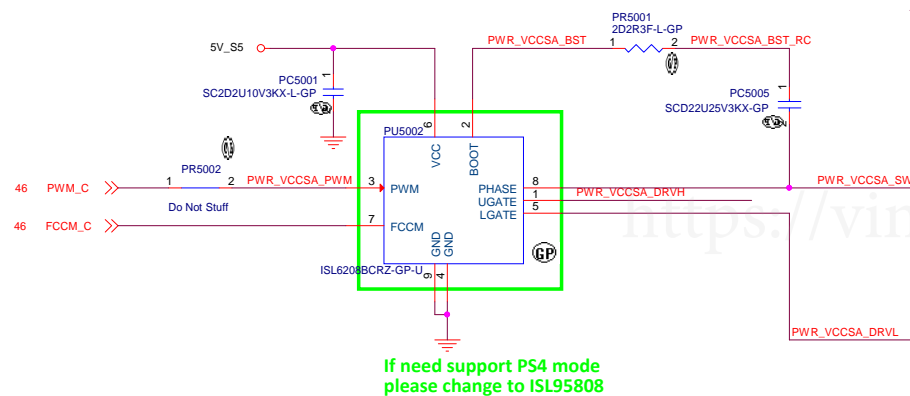
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved)		
Size A4	Document Number LS720	Rev -1N
Date: Friday, November 10, 2017	Sheet 49 of	115

```
Main Func = CPU_CORE
```

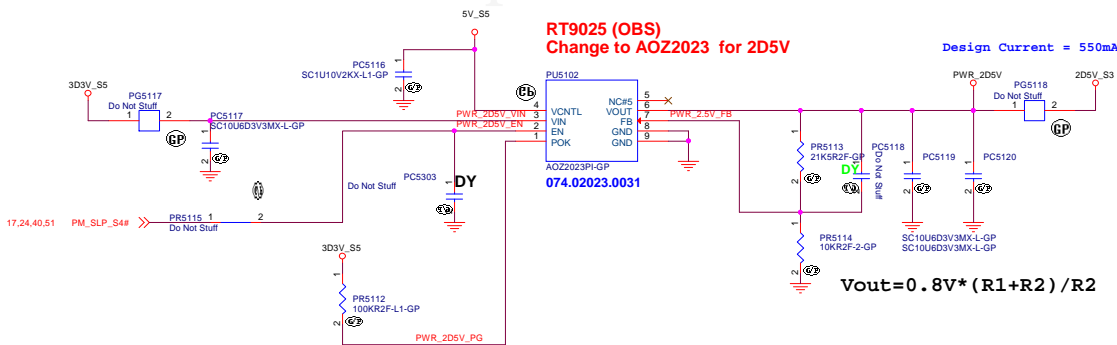
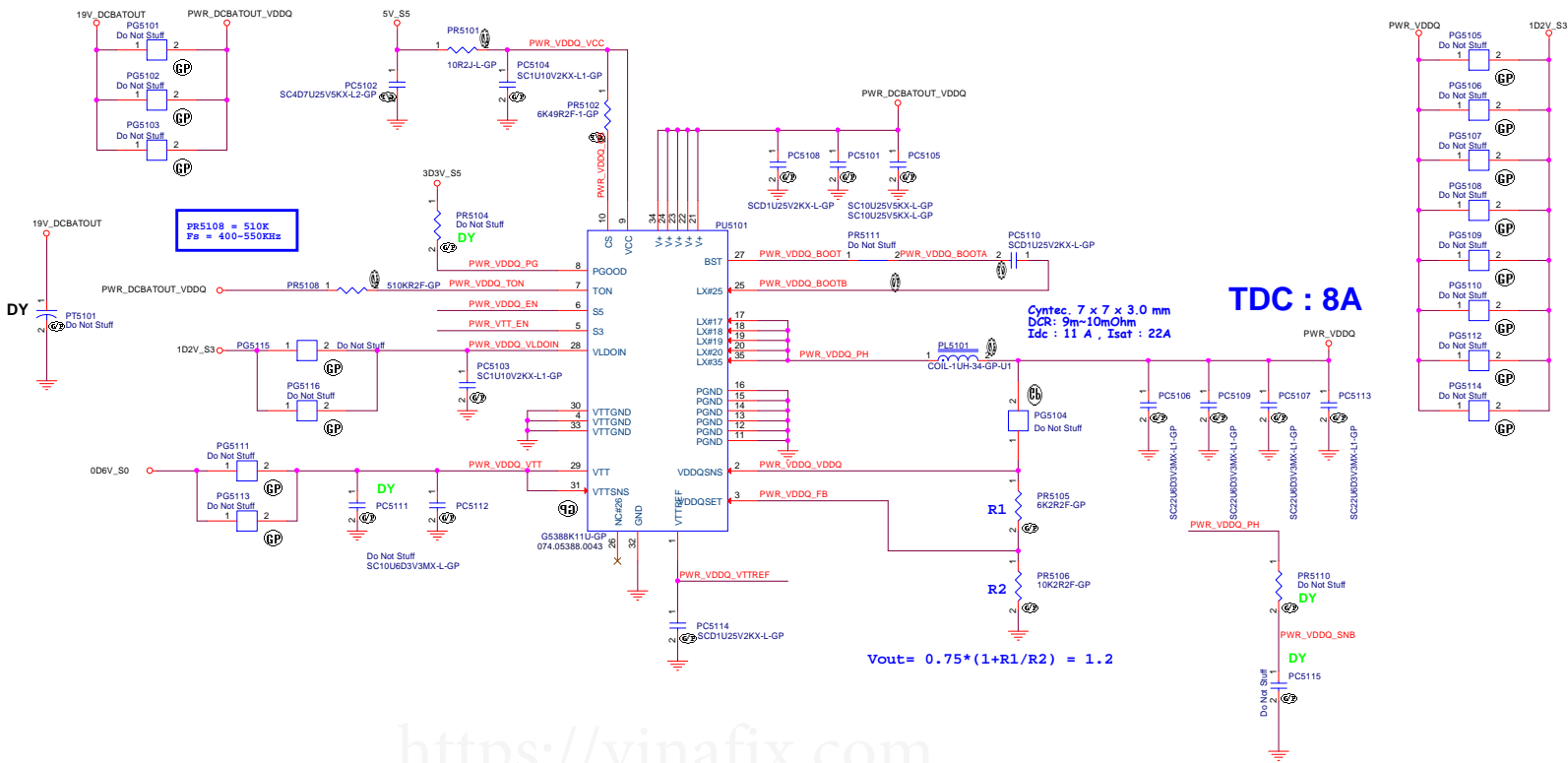
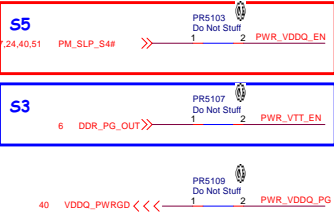


SKL\_H42\_45W  
Icc(max)=11.1A  
TDC=10A

Confirm with EE  
22uF/0805 total 10pcs  
(78.22610.L2L)



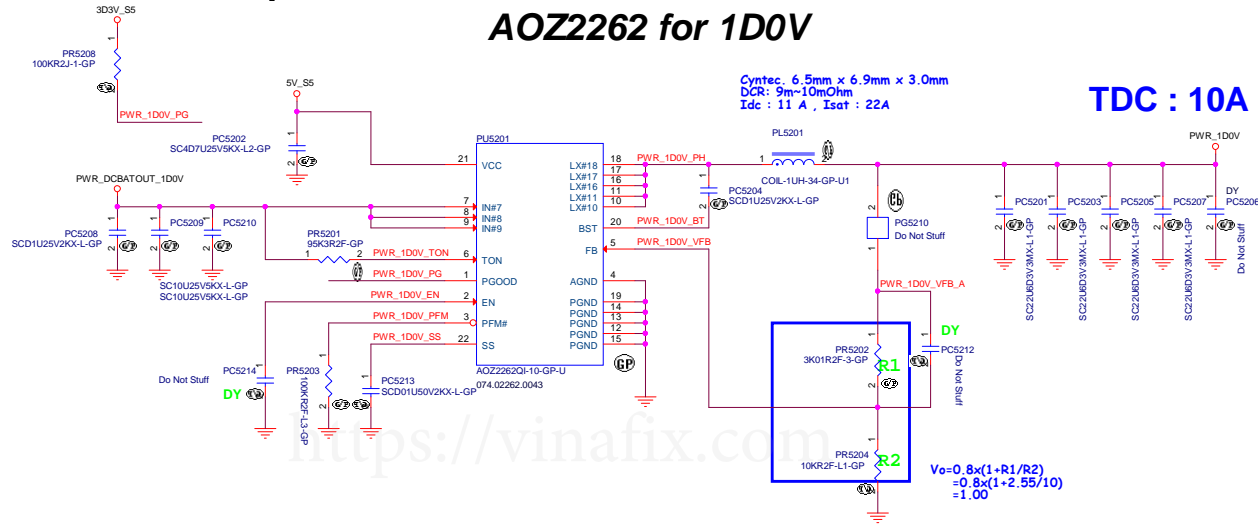
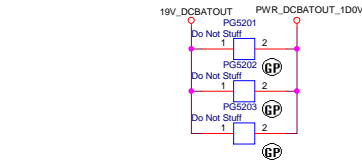
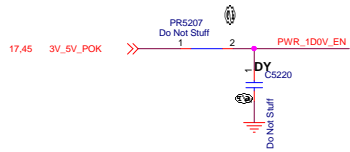
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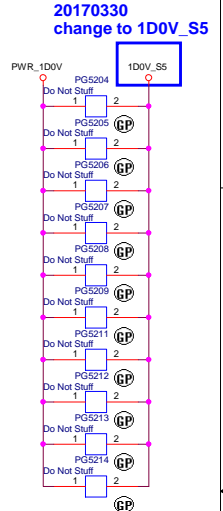
LS720 BOM		Wistron Corporation	
File		21F, 80, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Size		G5388 VDDQ	
Custom		LS720	
Date: Friday, November 10, 2017		Sheet 51 of 115	
		Rev -1N	

OFFPAGE

SSID = PWR.Plane.Regulator\_1p0v



COM	IC	AOZ2262(10A)	AOZ2261(8A)	AOZ2260(6A)
Chock		068.1R010.2121 IDC : 18A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP		22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1



LS720 BOM

**緯創資通 Wistron Corporation**  
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AOZ2262 1D0V**

Size: Custom Document Number: **LS720** Rev: **-1N**

Date: Friday, November 10, 2017 Sheet: 52 of 115

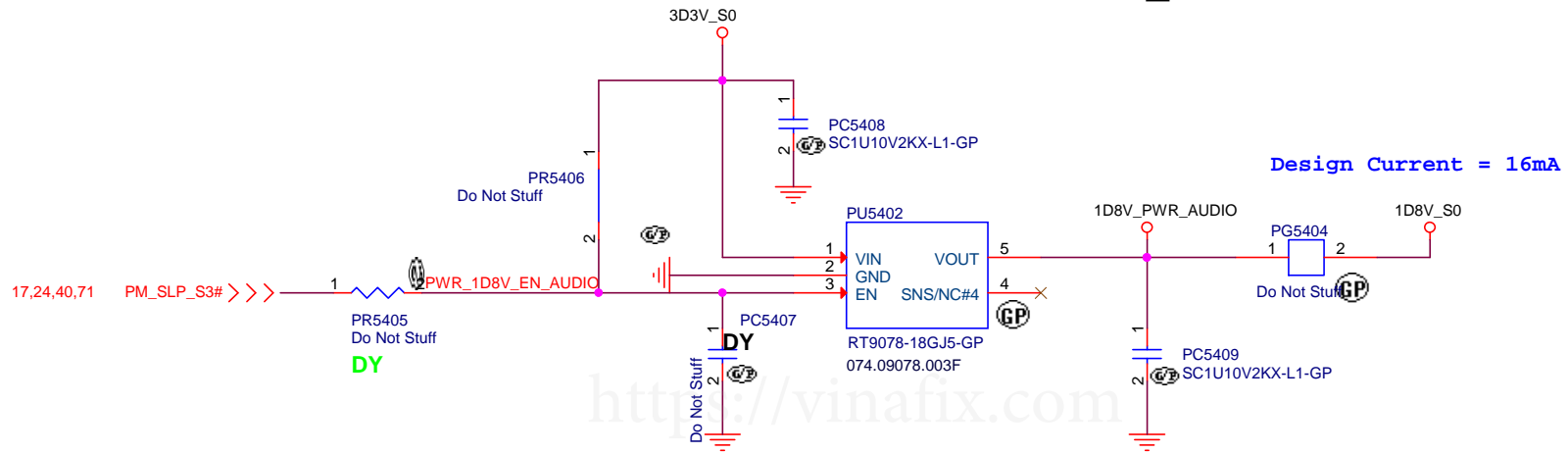
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LS720 BOM

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Size A4	Document Number <b>LS720</b>				Rev <b>-1N</b>
Date:	Friday, November 10, 2017		Sheet	53	of 115

**S-1339D18for 1D8V\_S0**



LS720 BOM

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
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***1D8V***

Size  
A4

Document Number

## LS720

teknisi indonesia

Rev  
-1N

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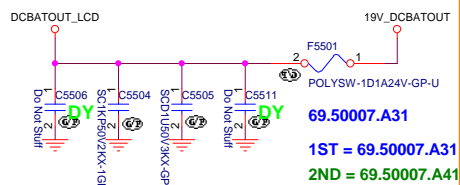
2

1
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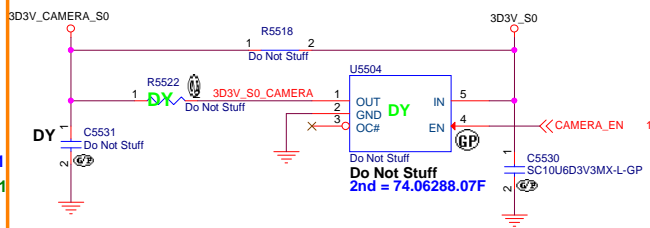
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**SSID = VIDEO**



*Layout 40 mil*      CAMERA POWER

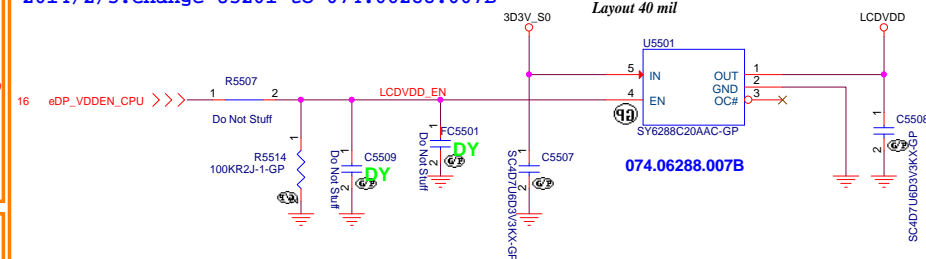


## SSID = VIDEO

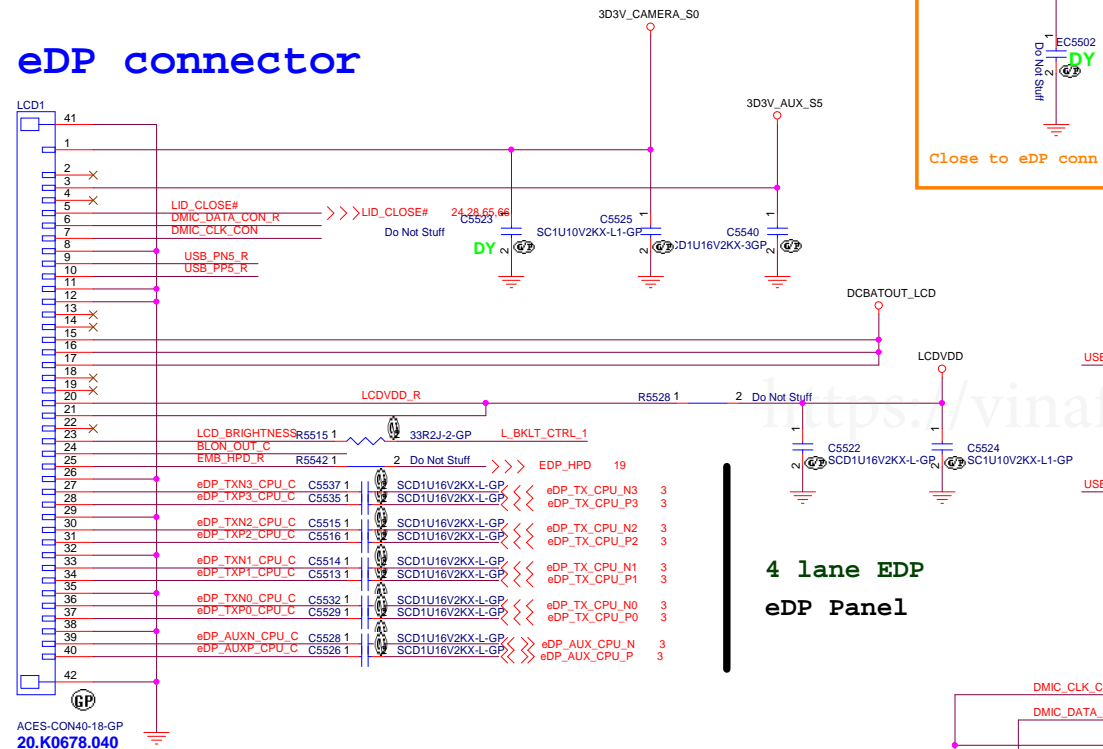
LCD POWER (Do Not use SW 74.09724.09F)

2014/2/5:Change U5201 to 074.06288.007B

*Layout 40 mil*



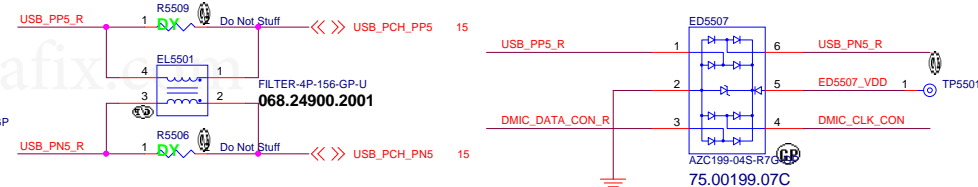
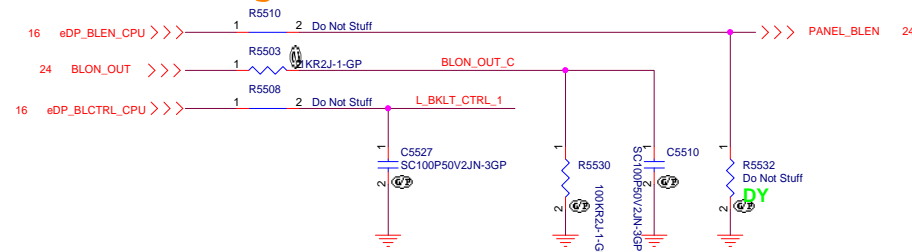
## eDP connector



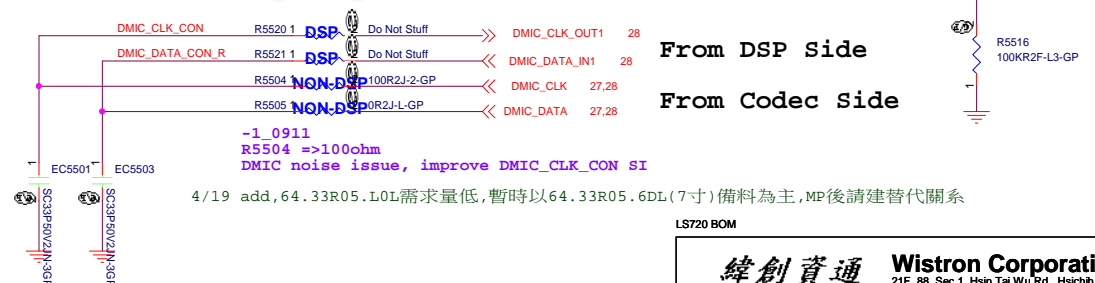
4 lane EDP

eDP Panel

## Panel BL brightness/Power En/BL En



SD\_DSP-&gt;DY\_0804



### From DSP Side

### From Codec Side

4/19 add, 64.33R05.L0L需求量低,暫時以64.33R05.6DL(7寸)備料為主,MP後請建替代關係

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Title **LCD&CAM&DMC&Touch**

Size A3	Document Number <b>LS720</b>	Rev <b>-1N</b>
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Title		
(Reserved)		
Size A4	Document Number LS720	Rev -1N
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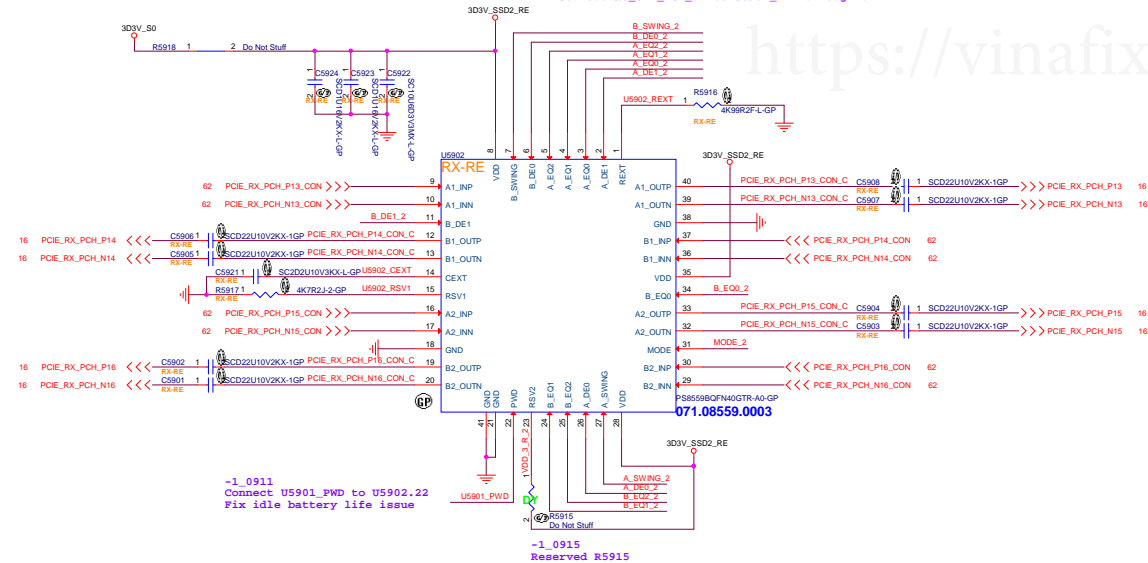
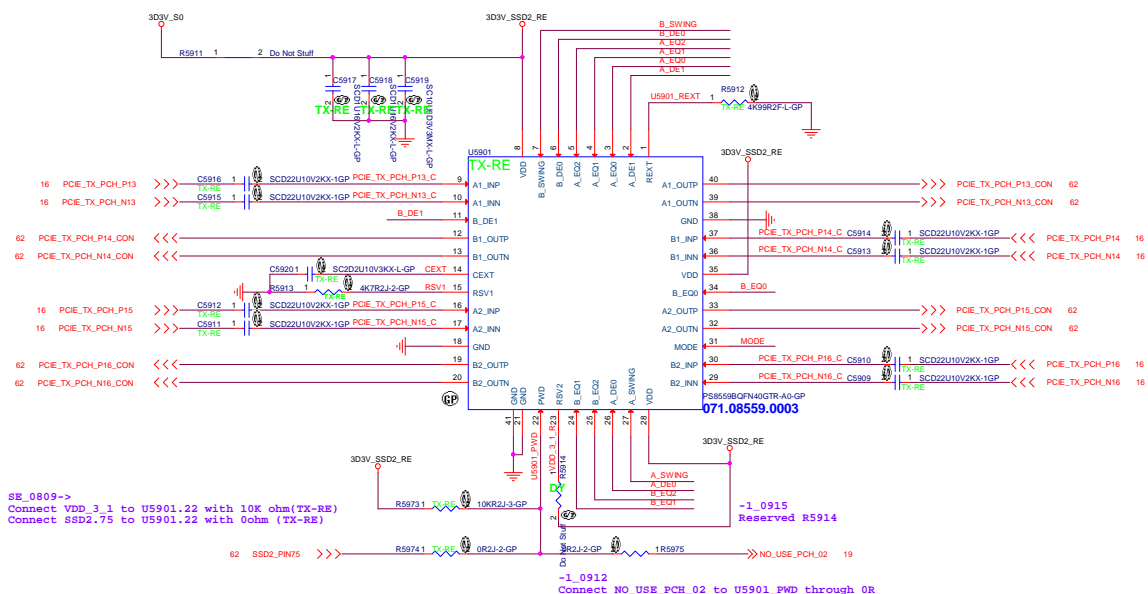
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title (RESERVED)		
Size A4	Document Number LS720	Rev -1N
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Title		
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R5960,R5961,R5962,R5963,R5964,R5965,R5969,R5972  
->DY for SSD2 IEMT test resault\_0802

Equalizer control and program for channel A.  
A\_EQ0, A\_EQ1 and A\_EQ2: internally pulled down at ~150K

A EQ<2:0>	EQ Level
000 (default)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

Equalizer control and program for channel B.  
B\_EQ0, B\_EQ1 and B\_EQ2: internally pulled down at ~150K

B_EQ<2:0>	EQ Level
000 (default)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

Programmable output de-emphasis level setting for channel A .  
A DE0 and A DE1: internally pulled down at ~150K

A DE<1:0>	DE Level
00(default)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB

Internally pulled down at  $\sim 150\text{K}\Omega$

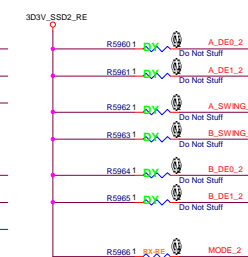
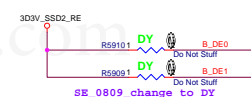
MODE	Operation Mode
0 (default)	SATA
1	PCIe

Program: programmable output de-emphasis level setting for channel B.  
B DE0 and B DE1: internally pulled down at ~150K

B_DE<1:0>	DE Level
00(default)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB

Internally pulled down at  $\sim 150\text{K}\Omega$

A_SWING	Swing Adjustment	B_SWING	Swing Adjustment
0 (default)	Default	0 (default)	Default
1	Increase 10%	1	Increase 10%



# BLANK

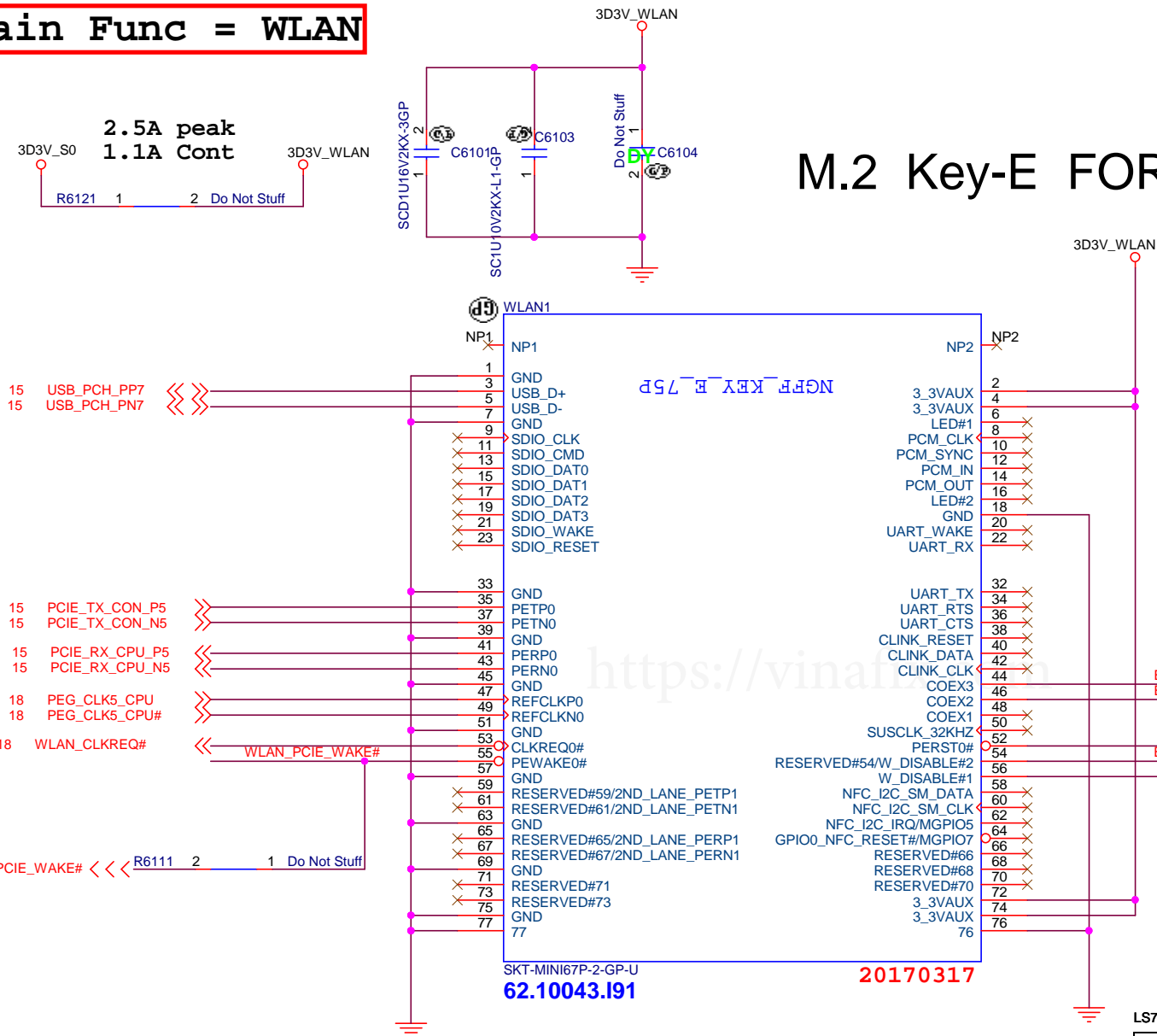
<https://vinafix.com>

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Title <b>SATA IF_HDD</b>			
Size A4	Document Number <b>LS720</b>		Rev <b>-1N</b>
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## Main Func = WLAN

## M.2 Key-E FOR WLAN / BT



LS720 BOM

緯創資通

# Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title
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## M.2 WLAN CONN

Size  
A4

Document Number
-----------------

# LS720

Rev	-1N
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## RF RESERVED



**Notes:**

- Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

18	1.5.0	0000	0000
22	1.5.0	0000	0000
26	10000120000100000100	0000	0000
30		0000	0000
34	Connective Key	Connective Key	Connective Key
38	Connective Key	Connective Key	Connective Key
42	Connective Key	Connective Key	Connective Key
46	N/C	N/C	N/C
50	16WARD (1000012.0) to N/C	0000	0000
54	CHARGE (1000012.0) to N/C	0000	0000
58	N/C	0000	0000
62	10001 (1000012.0) to N/C	0000	0000
66	N/C	0000	0000
70	10001 (1000012.0) to N/C	0000	0000
74	N/C	0000	0000
78	00001 (0)	0000	0000
82	N/C	0000	0000
86	N/C	0000	0000
90	N/C	0000	0000
94	N/C	0000	0000
98	N/C	0000	0000
102	N/C	0000	0000
106	N/C	0000	0000
110	N/C	0000	0000
114	N/C	0000	0000
118	N/C	0000	0000
122	N/C	0000	0000
126	N/C	0000	0000
130	N/C	0000	0000
134	N/C	0000	0000
138	N/C	0000	0000
142	N/C	0000	0000
146	N/C	0000	0000
150	N/C	0000	0000
154	N/C	0000	0000
158	N/C	0000	0000
162	N/C	0000	0000
166	N/C	0000	0000
170	N/C	0000	0000
174	N/C	0000	0000
178	N/C	0000	0000
182	N/C	0000	0000
186	N/C	0000	0000
190	N/C	0000	0000
194	N/C	0000	0000
198	N/C	0000	0000
202	N/C	0000	0000
206	N/C	0000	0000
210	N/C	0000	0000
214	N/C	0000	0000
218	N/C	0000	0000
222	N/C	0000	0000
226	N/C	0000	0000
230	N/C	0000	0000
234	N/C	0000	0000
238	N/C	0000	0000
242	N/C	0000	0000
246	N/C	0000	0000
250	N/C	0000	0000
254	N/C	0000	0000
258	N/C	0000	0000
262	N/C	0000	0000
266	N/C	0000	0000
270	N/C	0000	0000
274	N/C	0000	0000
278	N/C	0000	0000
282	N/C	0000	0000
286	N/C	0000	0000
290	N/C	0000	0000
294	N/C	0000	0000
298	N/C	0000	0000
302	N/C	0000	0000
306	N/C	0000	0000
310	N/C	0000	0000
314	N/C	0000	0000
318	N/C	0000	0000
322	N/C	0000	0000
326	N/C	0000	0000
330	N/C	0000	0000
334	N/C	0000	0000
338	N/C	0000	0000
342	N/C	0000	0000
346	N/C	0000	0000
350	N/C	0000	0000
354	N/C	0000	0000
358	N/C	0000	0000
362	N/C	0000	0000
366	N/C	0000	0000
370	N/C	0000	0000
374	N/C	0000	0000
378	N/C	0000	0000
382	N/C	0000	0000
386	N/C	0000	0000
390	N/C	0000	0000

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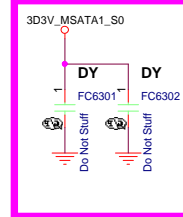
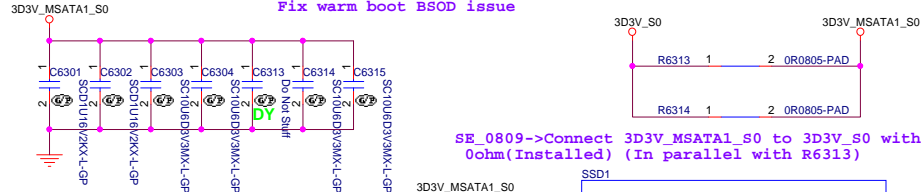
Title				<b>NGFF_mSATA_2</b>			
Size A3	Document Number						Rev
	<b>LS720</b>						<b>-1N</b>
Date:	Friday, November 10, 2017			Sheet	62	of	115

# (NGFF PCIE SSD)

-1\_0911

Add 10u caps \* 2 at 3D3V\_MSATA1\_S0  
Fix warm boot BSOD issue

RF RESERVED



18 MSATA\_CLKREQ\_CPU#  
14,24,61,62,66,68,71,79 PLT\_RST#

R6305 2 1 Do Not Stuff

MSATA\_RST#

3D3V\_MSATA1\_S0

SSD1

NP2

76

74

3\_3VAUX

72

3\_3VAUX

70

3\_3VAUX

68

SUSCLK\_32KHZ

58

NC#58

56

NC#56

54

PEWAKE#NC#54

52

CLKREQ#NC#52

50

PERST#NC#50

48

NC#48

46

NC#46

44

NC#44

42

NC#42

40

NC#40

38

DEVSLP

36

NC#36

34

NC#34

32

NC#32

30

NC#30

28

NC#28

26

NC#26

24

NC#24

22

NC#22

20

NC#20

18

3\_3VAUX

16

3\_3VAUX

14

3\_3VAUX

12

3\_3VAUX

10

DAS/DSS#

8

NC#8

6

NC#6

4

3\_3VAUX

2

3\_3VAUX

NGFF\_KEY\_M\_75P

SKT-MINI67P-1-GP-U  
62.10043.J01

20150528 change PN

Change EC6302 (78.33034.1FL->33pF/50V) to TVS diode ED6301 (PN:83.0005V.CAF)

-1\_0912

ED6301 ASM

Table 34-5. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

#### Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

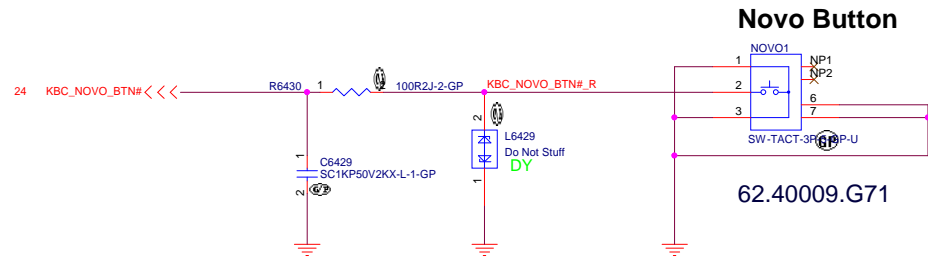
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	TXP	TXP	75	TXN
72	TXP	TXP	73	TXN
70	TXP	TXP	71	TXN
68	TXP	TXP	69	TXN
66	TXP	TXP	67	TXN
64	TXP	TXP	65	TXN
62	TXP	TXP	63	TXN
60	TXP	TXP	61	TXN
58	TXP	TXP	59	TXN
56	TXP	TXP	57	TXN
54	TXP	TXP	55	TXN
52	TXP	TXP	53	TXN
50	TXP	TXP	51	TXN
48	TXP	TXP	49	TXN
46	TXP	TXP	47	TXN
44	TXP	TXP	45	TXN
42	TXP	TXP	43	TXN
40	TXP	TXP	41	TXN
38	TXP	TXP	39	TXN
36	TXP	TXP	37	TXN
34	TXP	TXP	35	TXN
32	TXP	TXP	33	TXN
30	TXP	TXP	31	TXN
28	TXP	TXP	29	TXN
26	TXP	TXP	27	TXN
24	TXP	TXP	25	TXN
22	TXP	TXP	23	TXN
20	TXP	TXP	21	TXN
18	TXP	TXP	19	TXN
16	TXP	TXP	17	TXN
14	TXP	TXP	15	TXN
12	TXP	TXP	13	TXN
10	TXP	TXP	11	TXN
8	TXP	TXP	9	TXN
6	TXP	TXP	7	TXN
4	TXP	TXP	5	TXN
2	TXP	TXP	3	TXN

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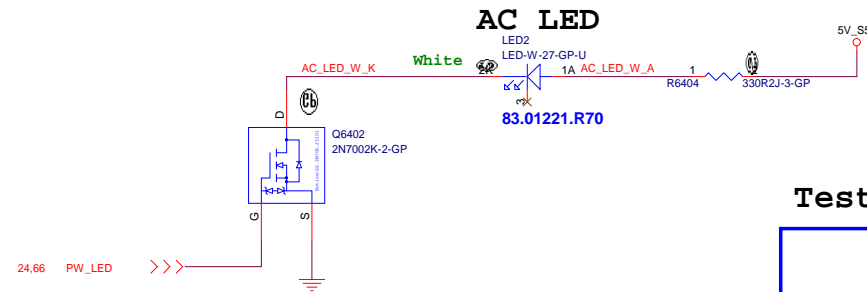
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title		NGFF_mSATA_1	
Size	Document Number	LS720	Rev -1N
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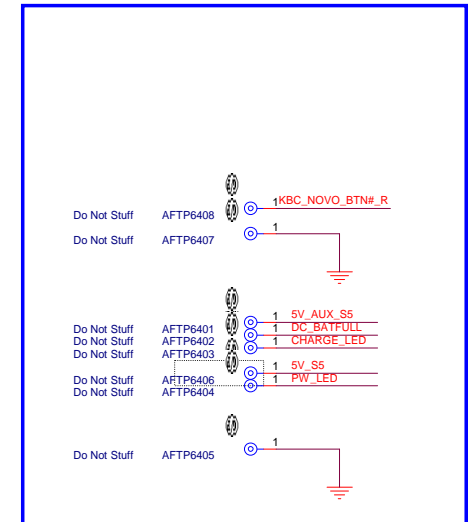


Vinafix.com

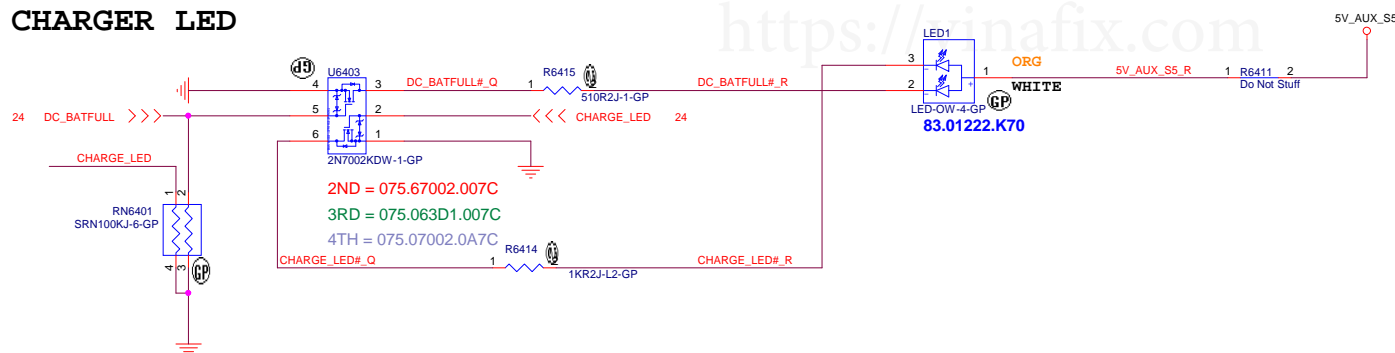
20170416 Need Check LED Definition in MB and Small BD



Test point



## CHARGER LED



## Electro-Optical Characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	V <sub>F</sub>	1.7	-----	2.3	V	I <sub>F</sub> =5mA
	T <sub>3</sub>	2.7	-----	3.3		

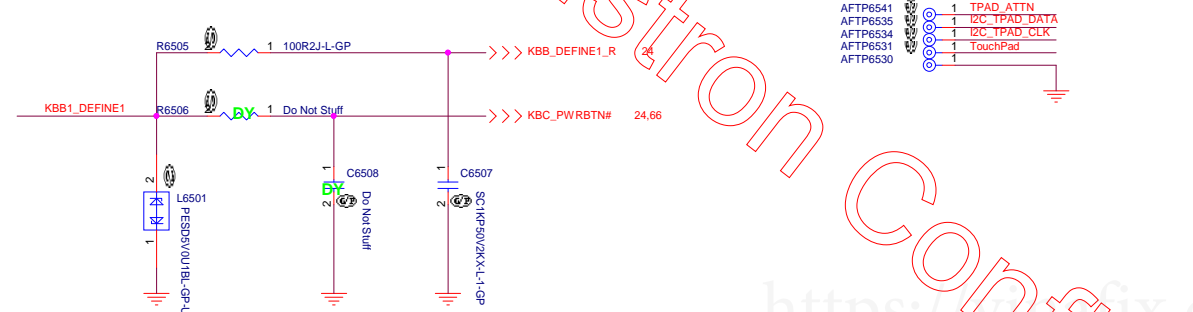
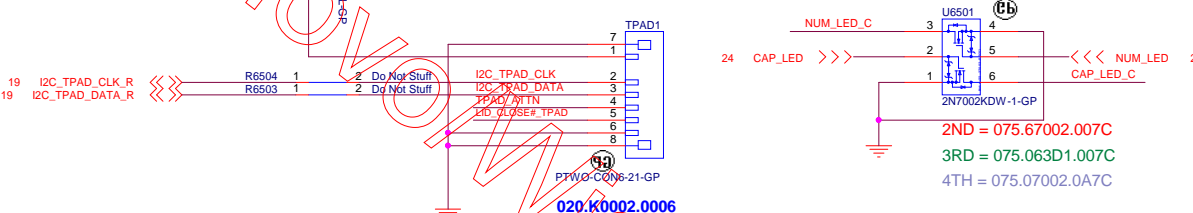
Chip Materials	Emitted Color
AlGaInP	Brilliant Orange
InGaN	Pure White

LS720 BOM

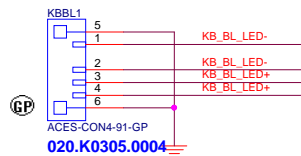
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>LED Board&amp;Power Button</b>	
Size: A3	Document Number: <b>LS720</b>
Date: Friday, November 10, 2017	Rev: <b>-1N</b>
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SSID = Touch.Pad

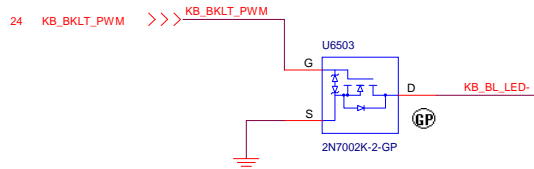


## Keyboard Backlight CN

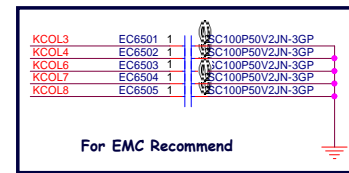


6/18 KBL1 KB\_BL\_LED+ 與 KBL1 KB\_BL\_LED- 互換  
10/6 KBL1 add 2nd source

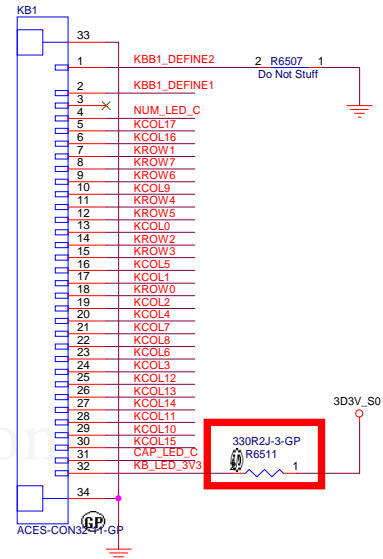
U6203 Keyboard Backlight U6203&BLKB1:



07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31



## Internal KeyBoard Connector



CAP_LED_C	1	AFTP6537	Do Not Stuff
KB_LED_3V3	1	AFTP6536	Do Not Stuff
KCOL15	1	AFTP6501	Do Not Stuff
KCOL10	1	AFTP6502	Do Not Stuff
KCOL11	1	AFTP6503	Do Not Stuff
KCOL14	1	AFTP6504	Do Not Stuff
KCOL13	1	AFTP6505	Do Not Stuff
KCOL12	1	AFTP6506	Do Not Stuff
KCOL3	1	AFTP6507	Do Not Stuff
KCOL8	1	AFTP6508	Do Not Stuff
KCOL7	1	AFTP6509	Do Not Stuff
KCOL4	1	AFTP6510	Do Not Stuff
KCOL2	1	AFTP6511	Do Not Stuff
KROW0	1	AFTP6512	Do Not Stuff
KCOL1	1	AFTP6513	Do Not Stuff
KCOL5	1	AFTP6514	Do Not Stuff
KROW2	1	AFTP6515	Do Not Stuff
KROW3	1	AFTP6516	Do Not Stuff
KROW4	1	AFTP6517	Do Not Stuff
KROW5	1	AFTP6518	Do Not Stuff
KROW6	1	AFTP6519	Do Not Stuff
KROW7	1	AFTP6520	Do Not Stuff
KCOL9	1	AFTP6521	Do Not Stuff
KCOL16	1	AFTP6522	Do Not Stuff
KCOL17	1	AFTP6523	Do Not Stuff
NUM_LED_C	1	AFTP6524	Do Not Stuff
NUM_LED_C	1	AFTP6540	Do Not Stuff
NUM_LED_C	1	AFTP6539	Do Not Stuff
NUM_LED_C	1	AFTP6538	Do Not Stuff

AFTP6501-AFTP6525  
CLOSE keyboard connector  
20150602 change PN

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Title		
<b>Key Board&amp;Touch Pad</b>		
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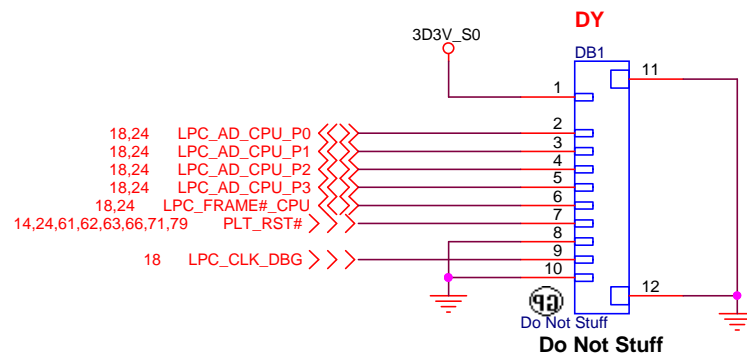


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Title					
<b>(RESERVED)</b>					
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<b>Debug connector</b>	
Size A4	Document Number <b>LS720</b>
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<https://vinafix.com>

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Title <b>RESERVED</b>		
Size A4	Document Number <b>LS720</b>	Rev <b>-1N</b>
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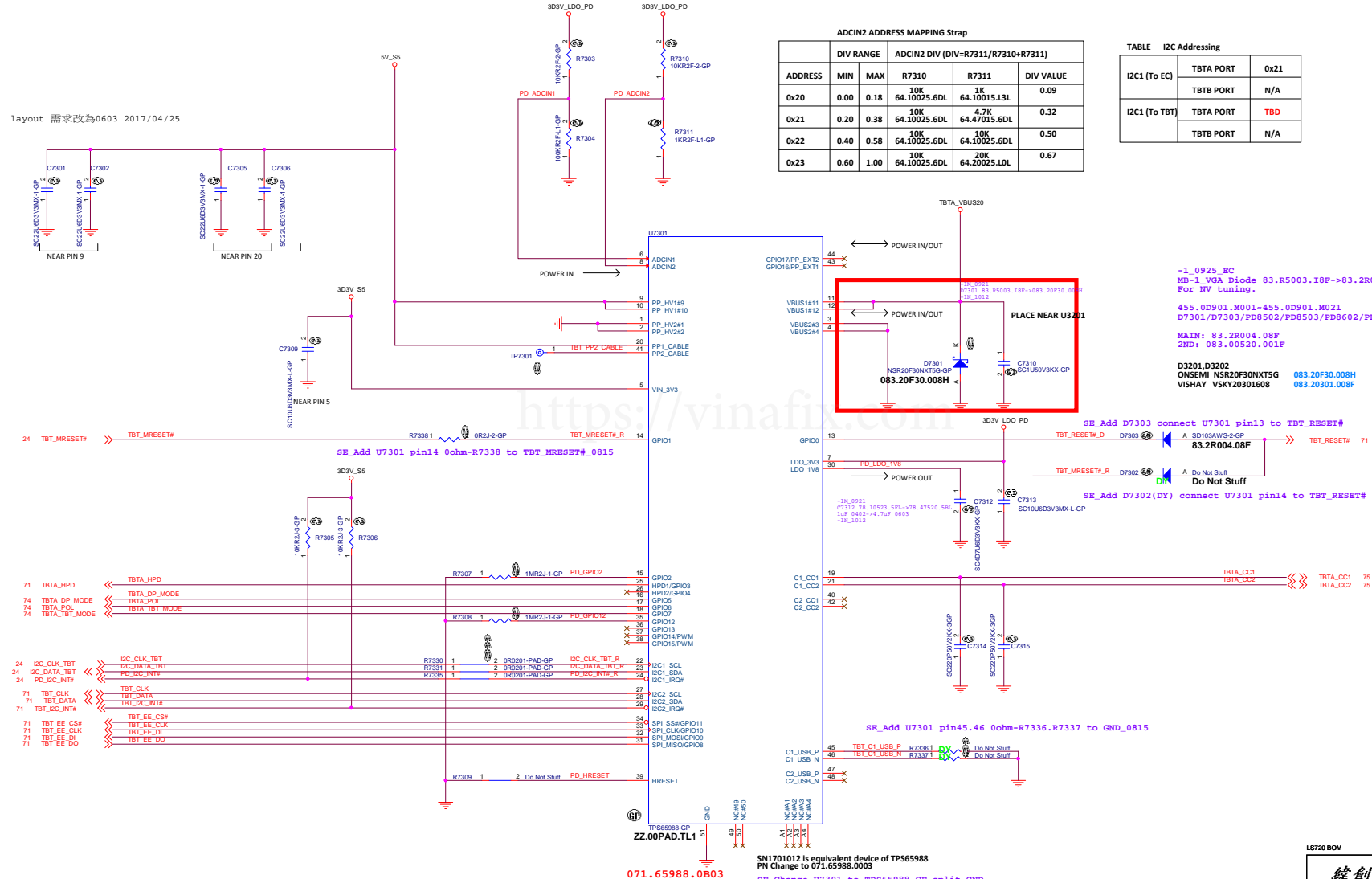


## ADCIN2

### Table 8. I<sup>2</sup>C Address Selection

DIV = R2/(R1+R2) <sup>(1)</sup>		I <sup>2</sup> C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR Decode_C1	I2C_ADDR Decode_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.



```

-1_0925_BC
MB-1_VGA_Diode 83.R5003.I8F->83.2R004.08F
For NV tuning.

455.D901.M001-455.D901.M021
D7301/D7303/PD8502/PD8503/PD8602/PD8603/PD8604/PD8606/PD8607/PD8608

MAIN: 83.2R004.08F
2ND: 083.00520.001F

D3201,D3202
ONSEMI NSR2030NXTS5 083.20F30.008H
VISHAY VSKY20301608 083.20301.008F

```

```
SE_Add D7303 connect U7301 pin13 to TBT_RESET#
```

```
SE_Add D7302(DY) connect U7301 pin14 to TBT_RESET#
```

```
SE_Add U7301 pin45.46 0ohm-R7336.R7337 to GND_0815
```

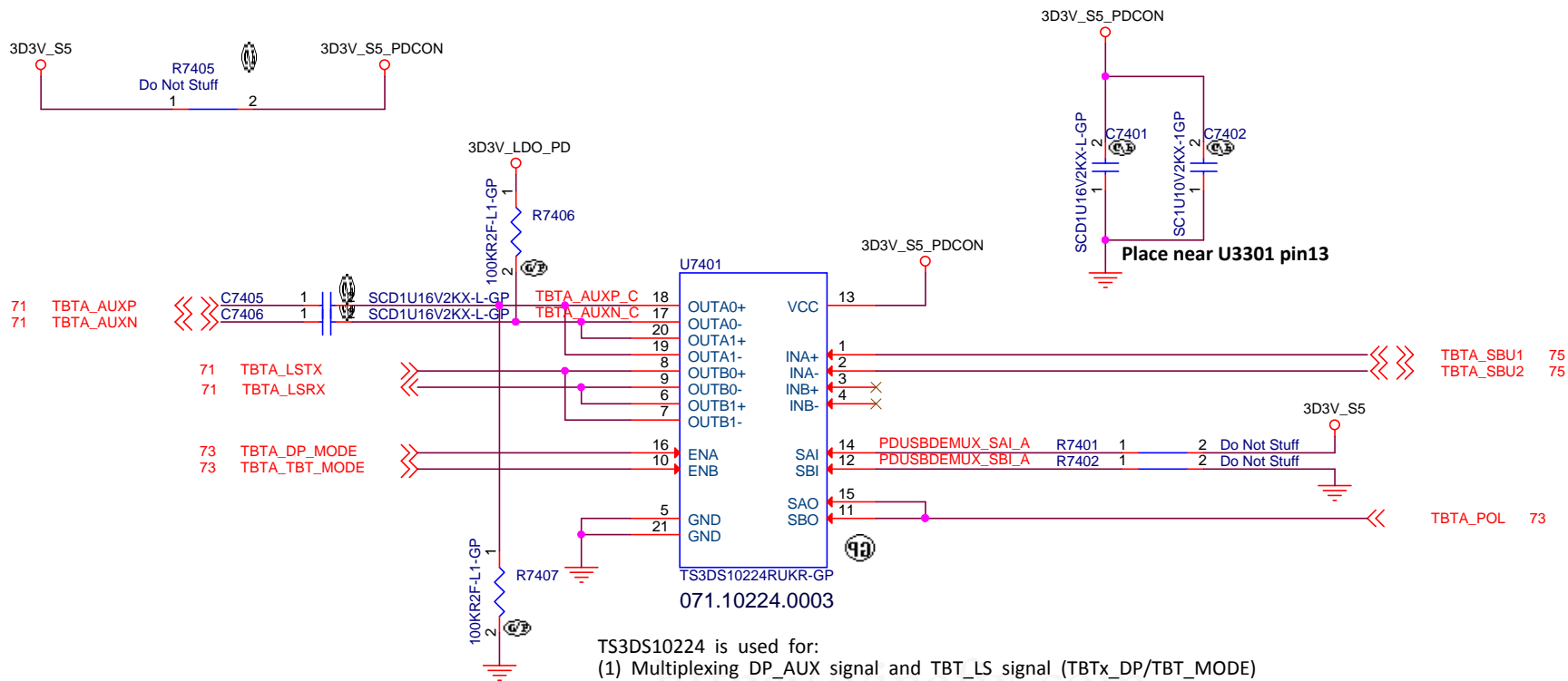
```
SN1701012 is equivalent device of TP565988
PN Change to 071.65988.0003

SE_Change U7301 to TP565988 CE split GND
version(Sync up with TPG project)_0808

PN Change from 074.17010.0073 to 071.65988.0A03

SE_PN Change from 071.65988.0A03 to ZZ.00PAD.TL1
sould BOM Ctrl !!!_0811
```

LS720 BOM		<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Thunderbolt(35)</b>			
Size A2	Document Number		Rev
	<b>LS720</b>		<b>-1N</b>
Date:	Friday, November 10, 2017	Sheet 73	of 115



TS3DS10224 is used for:  
 (1) Multiplexing DP\_AUX signal and TBT\_LS signal (TBTx\_DP/TBT\_MODE)  
 (2) Supporting cable flip. (TBTx\_POL)  
 Those function had been supported in TPS65982 but not in TPS65988/SN1701012

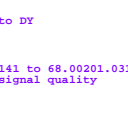
LS720 BOM

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Title	
<b>Thunderbolt(4/5)</b>	
Size A4	Document Number <b>LS720</b>
Date: Friday, November 10, 2017	Rev <b>-1N</b>

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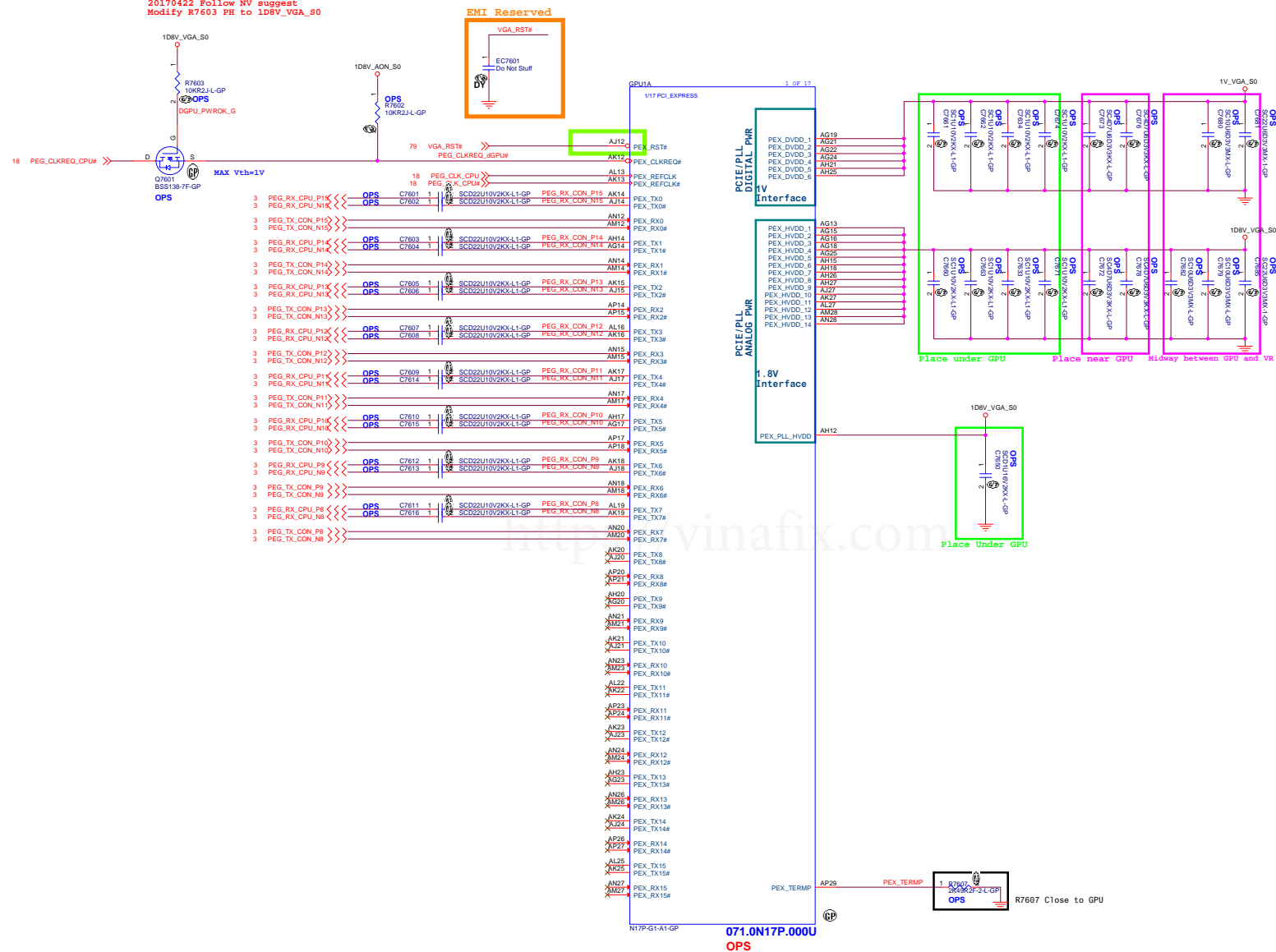


073.00331.0003  
073.07213.0003



- PEX\_HVDD and PEX\_PLL\_HVDD rails must be shared with 1V8\_AON for GC6 2.1

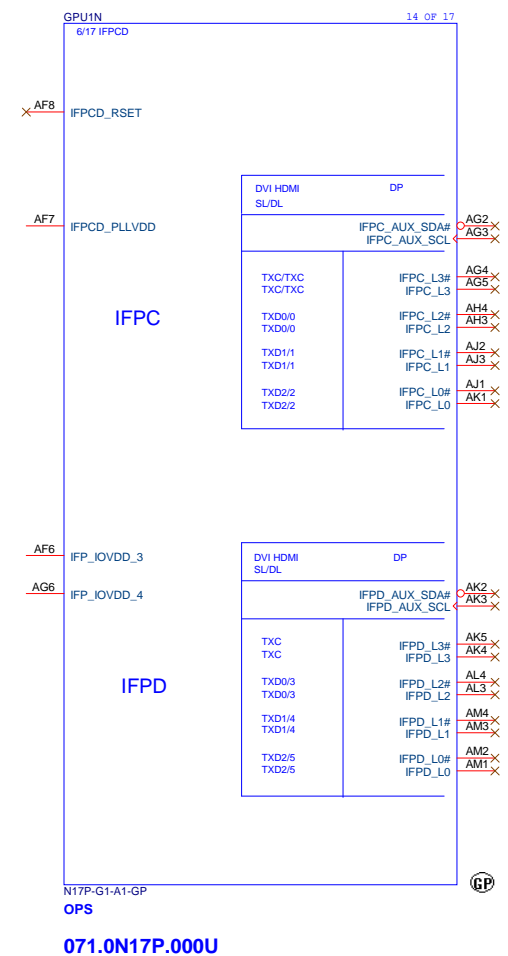
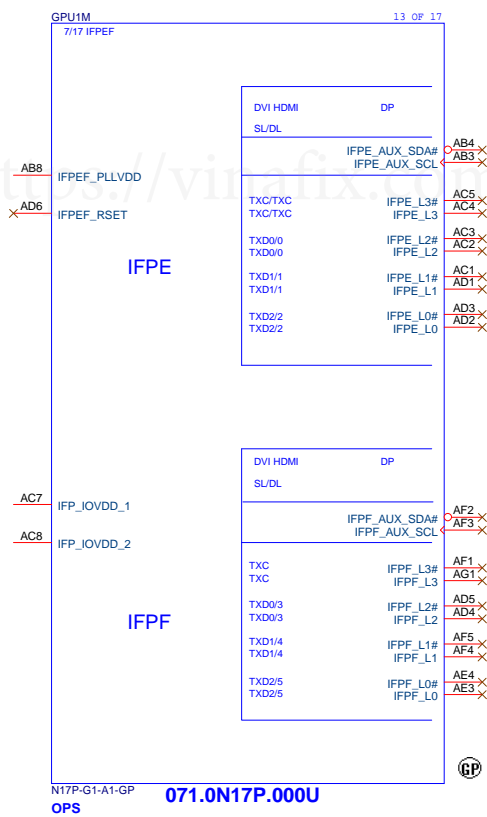
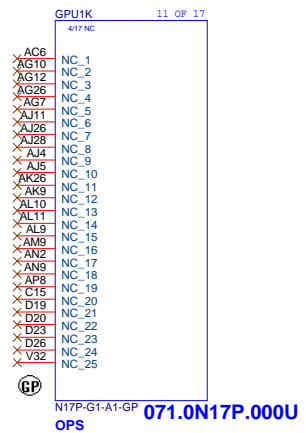
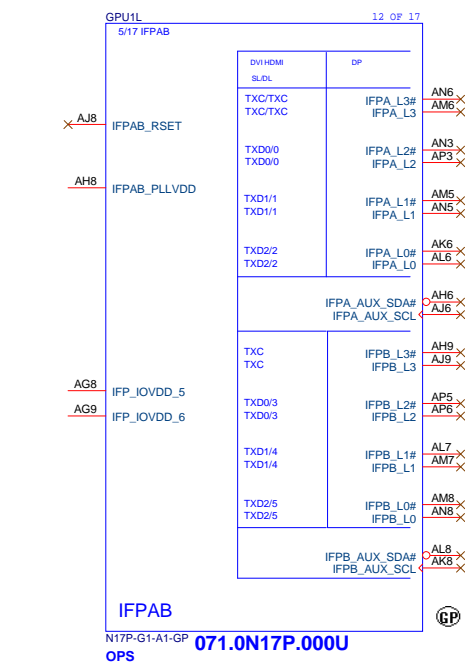
20170422 Follow NV suggest  
Modify R7603 PH to 1D8V\_VGA\_S0



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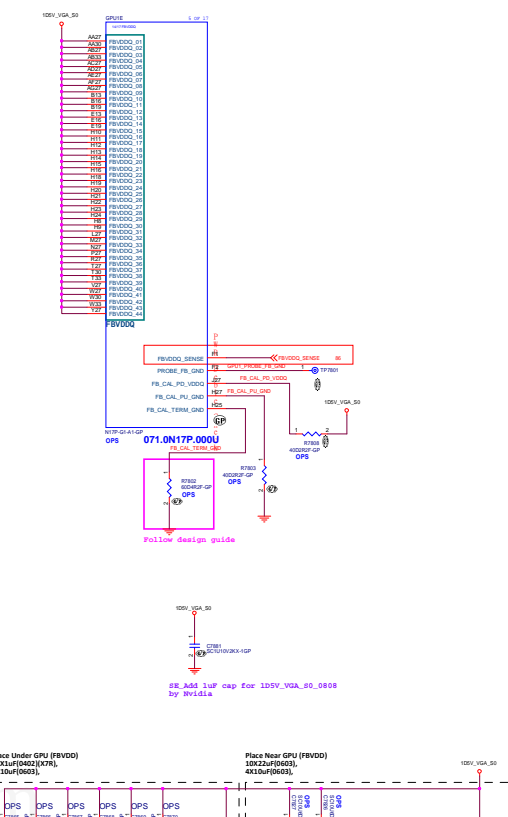
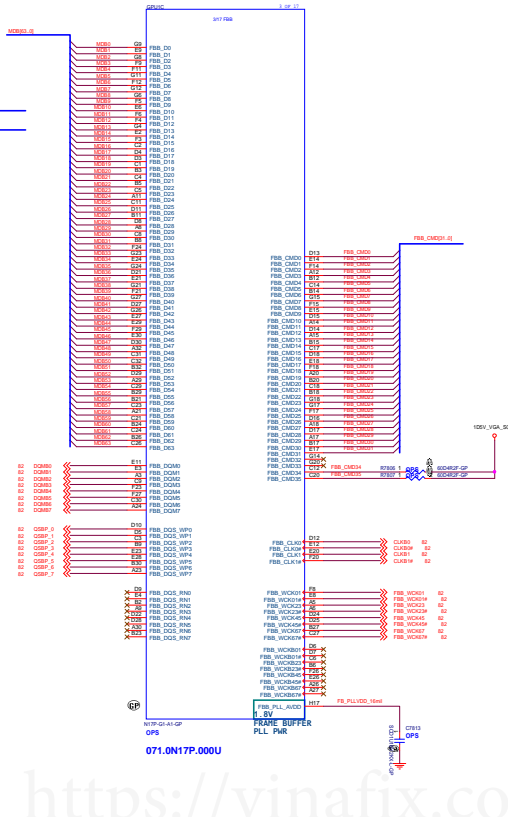
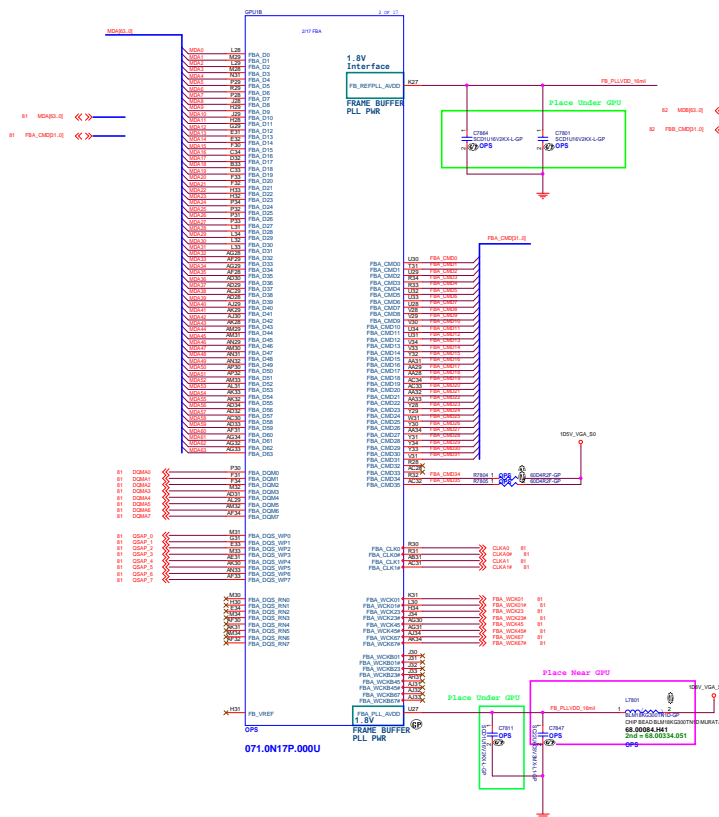
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,  
Taichung Hsien 421, Taiwan, R.O.C.

Title			
GPU 1050M PEG (1/5)			
Size A2	Document Number		Rev
	LS720		-1
Date	Friday, November 10, 2017	Sheet 76 of 116	



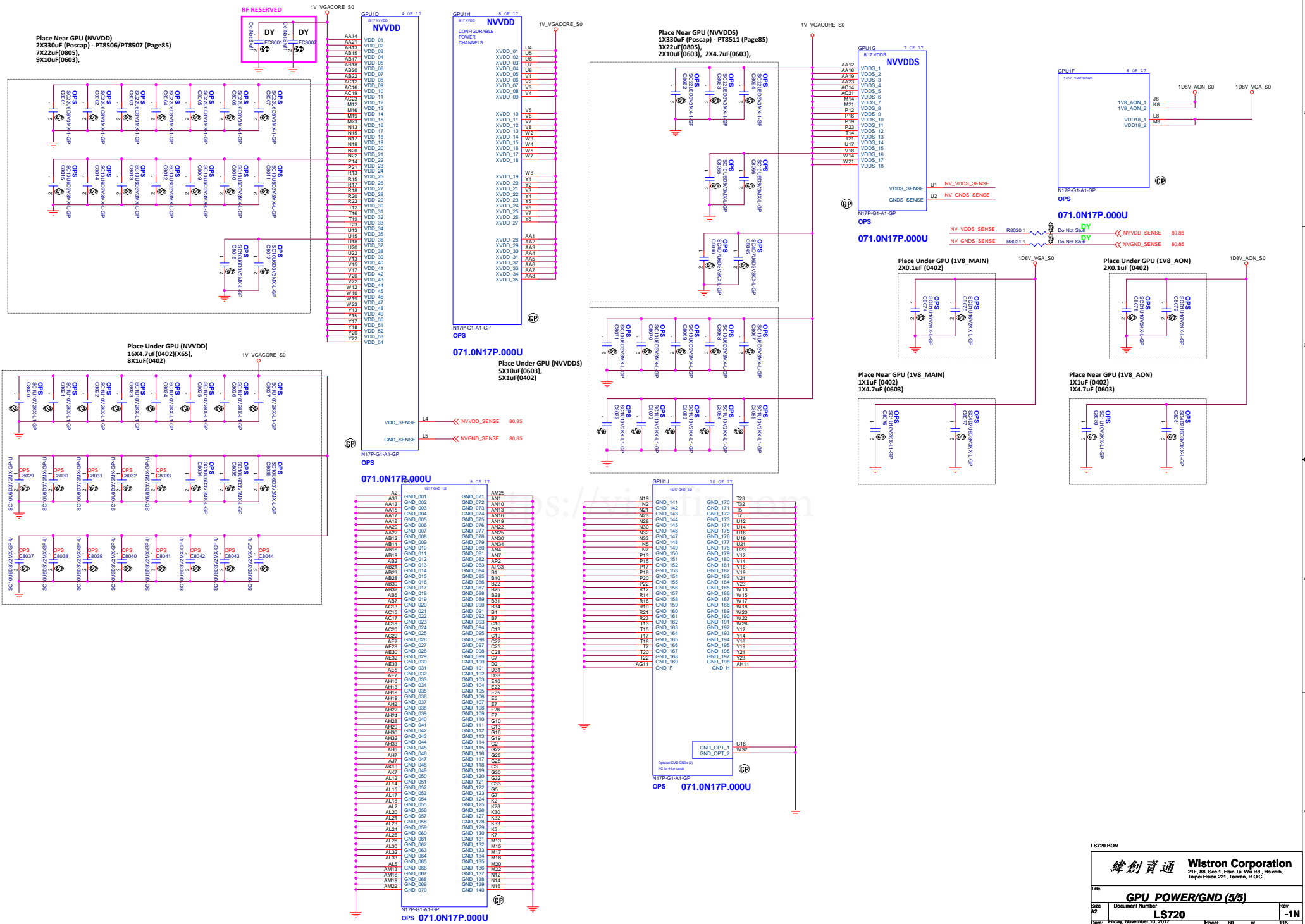
LS720 BOM

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU DIGITALOUT (2/5)</b>		
Size A3	Document Number <b>LS720</b>	Rev <b>-1N</b>
Date: Friday, November 10, 2017	Sheet 77 of 115	

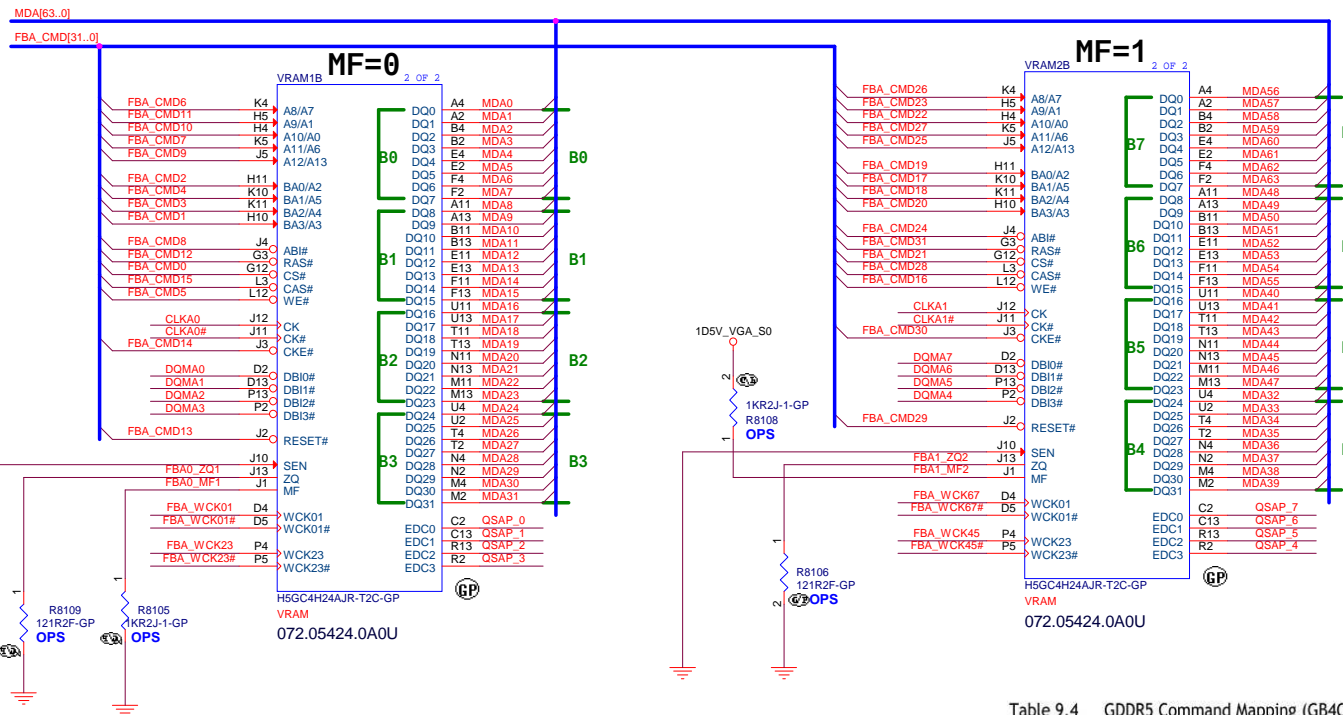




 <b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU GPIO/STRAP</b>			
Size A2	Document Number		Rev <b>-1</b>
<b>LS720</b>			
Date:	Friday, November 10, 2017	Sheet 79 of	115







GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)
GDDR5 CLK Mapping							
WCK01	WCK23 (WCK45)			WCK23	WCK01 (WCK67)		
WCK01#	WCK23# (WCK45#)			WCK23#	WCK01# (WCK67#)		
CK	CK						
CK#	CK#						
Others							
MF	MF	SEN	SEN				
ZQ	ZQ	RESET#	RESET#				

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

**VRAM 1,2 (1/4)**

Size

Document Number
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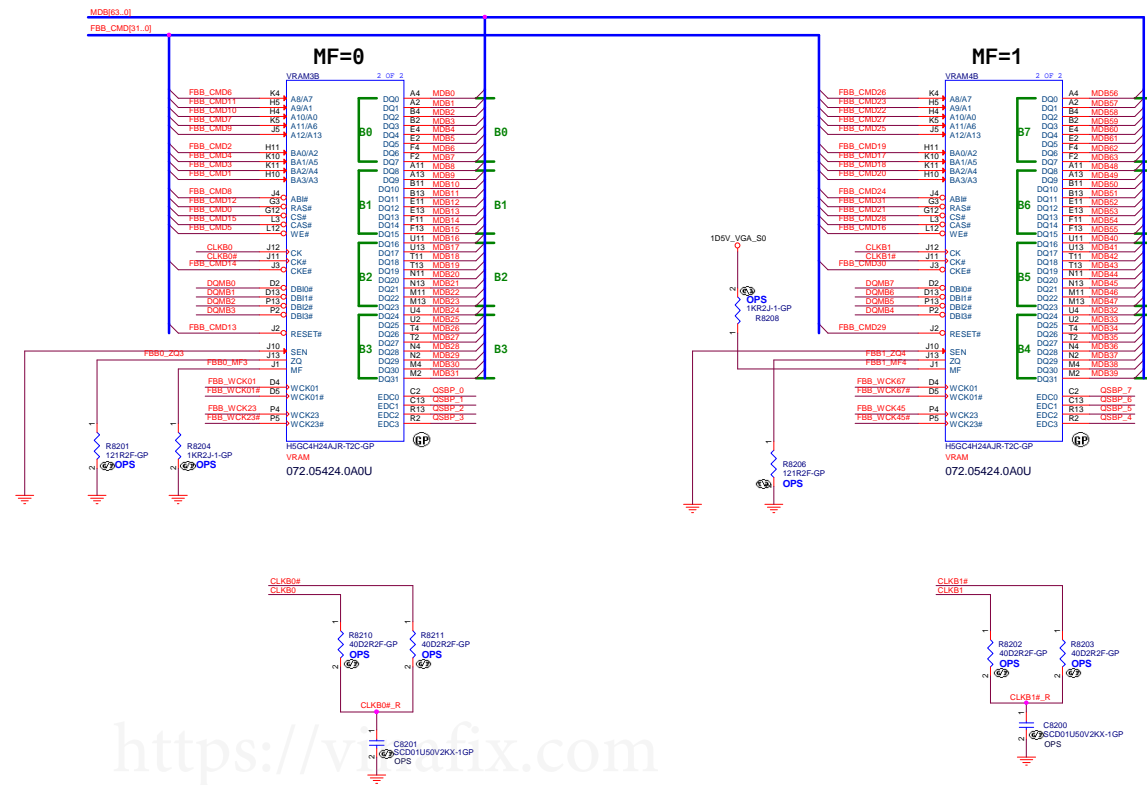
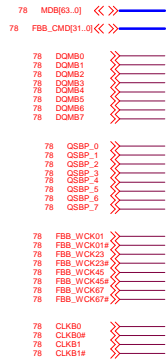
LS720

Date \_\_\_\_\_

Friday, November 10, 2017

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1



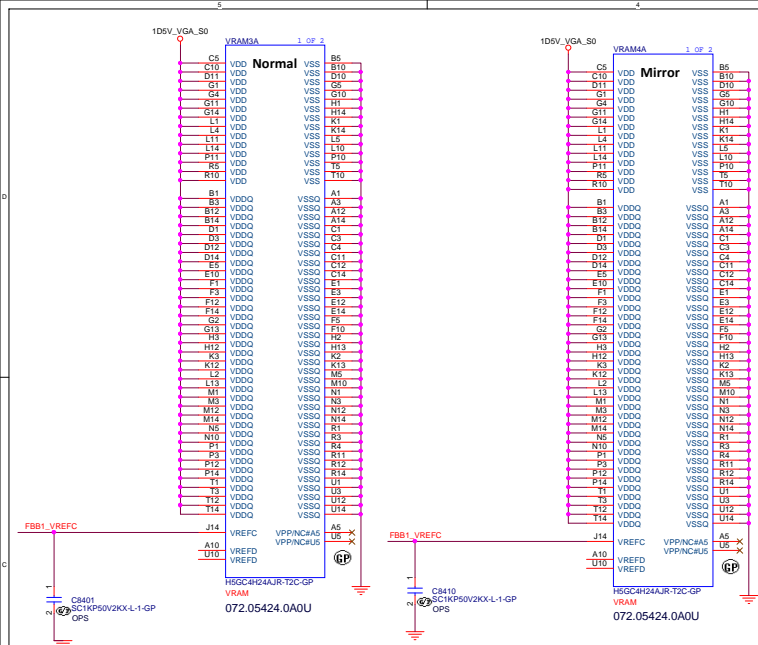
GDDR5 Data Mapping											
BYTE0 (BT0)			BYTE1 (BT1)			BYTE2 (BT2)			BYTE3 (BT3)		
MF=0	MF=1		MF=0	MF=1		MF=0	MF=1		MF=0	MF=1	
DQ0	DQ24 (DQ32)		DQ8	DQ16 (DQ48)		DQ16	DQ8 (DQ48)		DQ24	DQ0 (DQ32)	
DQ1	DQ25 (DQ33)		DQ9	DQ17 (DQ41)		DQ17	DQ9 (DQ45)		DQ25	DQ1 (DQ37)	
DQ2	DQ26 (DQ34)		DQ10	DQ18 (DQ42)		DQ18	DQ10 (DQ46)		DQ26	DQ2 (DQ38)	
DQ3	DQ27 (DQ35)		DQ11	DQ19 (DQ43)		DQ19	DQ11 (DQ47)		DQ27	DQ3 (DQ39)	
DQ4	DQ28 (DQ36)		DQ12	DQ20 (DQ44)		DQ20	DQ12 (DQ49)		DQ28	DQ4 (DQ40)	
DQ5	DQ29 (DQ37)		DQ13	DQ21 (DQ45)		DQ21	DQ13 (DQ51)		DQ29	DQ5 (DQ41)	
DQ6	DQ30 (DQ38)		DQ14	DQ22 (DQ46)		DQ22	DQ14 (DQ52)		DQ30	DQ6 (DQ42)	
DQ7	DQ31 (DQ39)		DQ15	DQ23 (DQ47)		DQ23	DQ15 (DQ53)		DQ31	DQ7 (DQ43)	
DBI0	DBI3 (DQ44)		DBI1	DBI2 (DQ45)		DBI2	DBI1 (DQ46)		DBI3	DBI0 (DQ47)	
EDC0	EDC3 (DQ48)		EDC1	EDC2 (DQ49)		EDC2	EDC1 (DQ50)		EDC3	EDC0 (DQ51)	
GDDR5 CLK Mapping											
WCK01	WCK23 (WCK45)		WCK23	WCK01 (WCK45)		WCK01#	WCK23# (WCK45)		WCK01#	WCK23# (WCK45)	
CK#	CK#		CK#	CK#		CK#	CK#		CK#	CK#	
Others											
MF	MF	SEN	SEN	RESET#	RESET#						
ZQ	ZQ										

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	DRAM Signal Definition
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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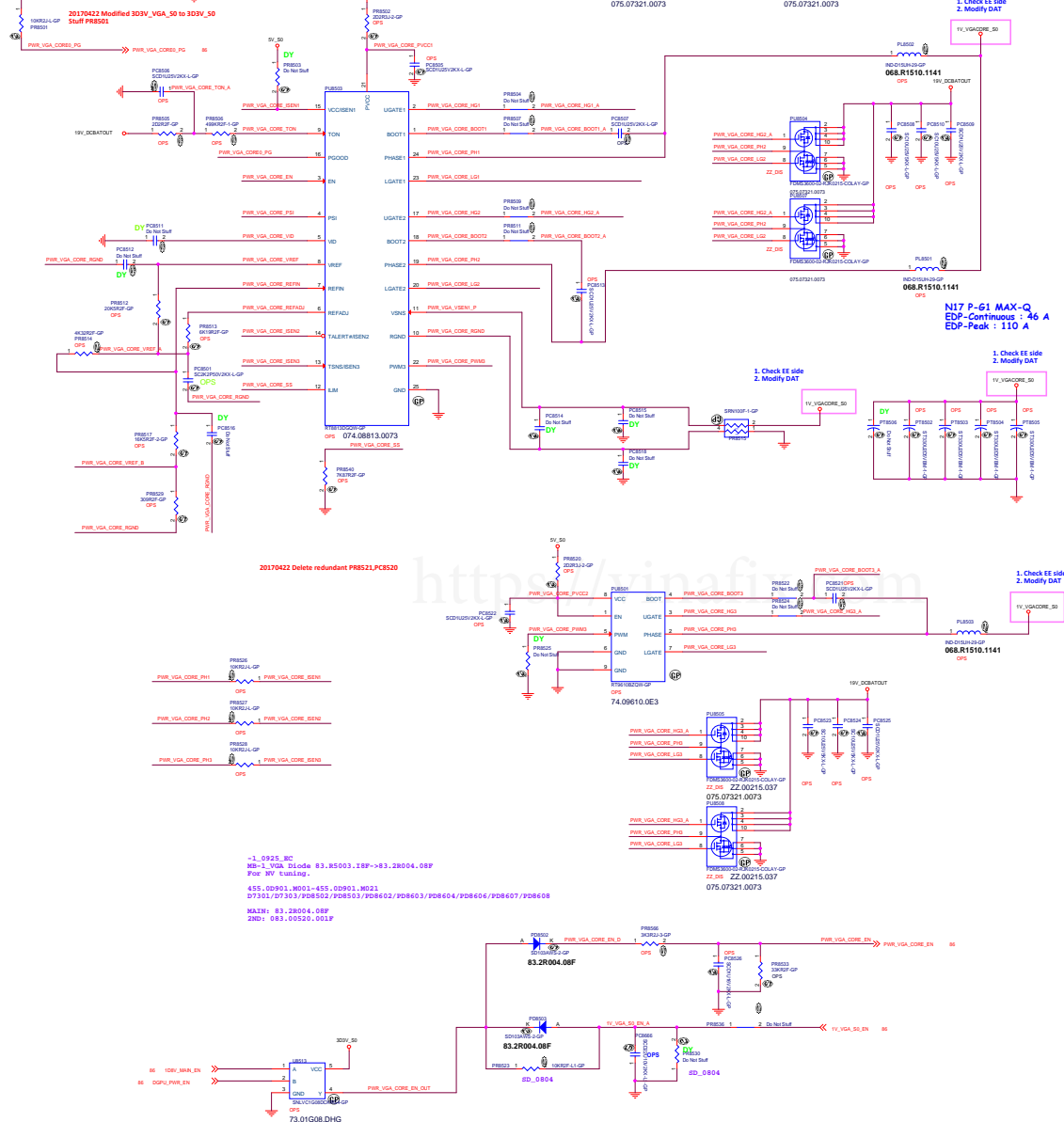


1. Check EE side



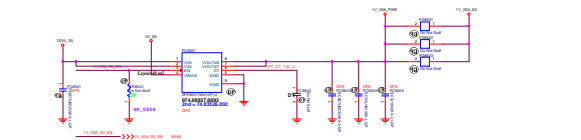
### PWM-VID Specification

Pin# Pin specification		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Step	mV	6.25
Number of Voltage Levels N	level	160
PWMI Frequency F <sub>pwmi</sub>	kHz	675
PWMI Minimum Pulse Width T <sub>pwmi</sub>	ns	9.24
VID Transient Time T	us	100
Component Value		
R1 (1%)	kΩ	6.19
R2 (1%)	kΩ	20.5
R3 (1%)	kΩ	4.32
R4 (1%)	kΩ	16.5
R5 (1%)	kΩ	0.209
C	nF	1.3

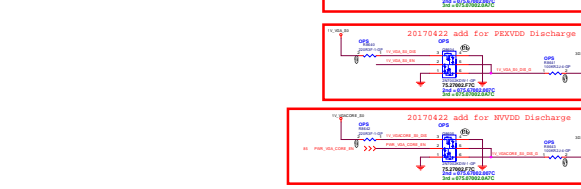
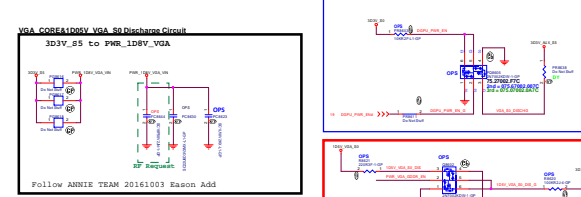
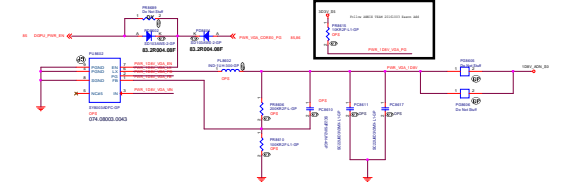


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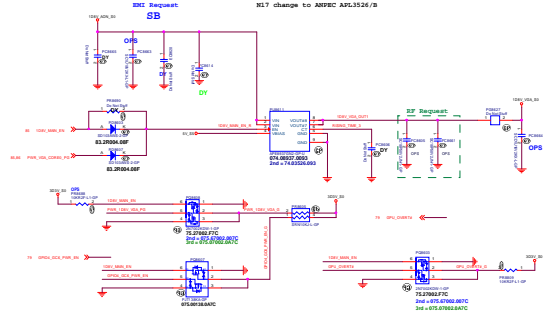
# APL3526QB for 1V\_VGA\_S0



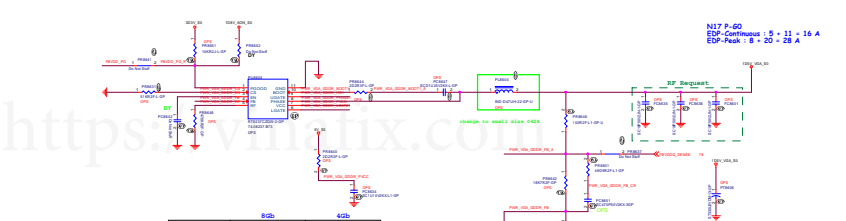
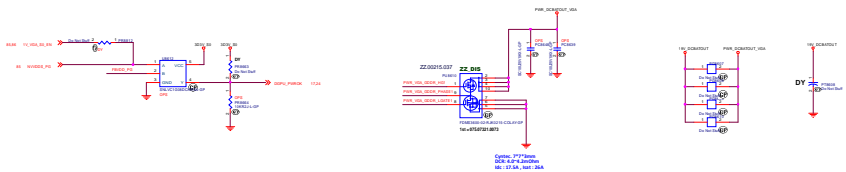
# SY8003A for PWR\_VGA\_1D8V



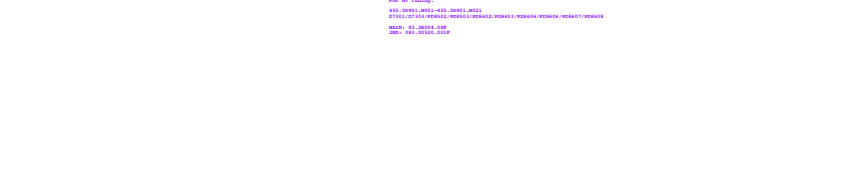
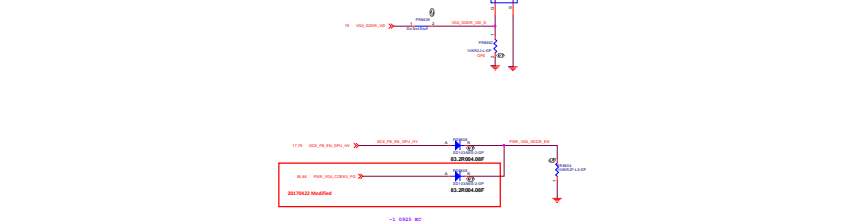
# SYW232 for 1D8V\_MAIN



# RT8816A for PWR\_VGA\_GDDR



VRAM TYPE_V	VRAM TYPE_V	VRAM TYPE_V
VRAM_TYPE_V	VRAM_TYPE_V	VRAM_TYPE_V
VRAM_TYPE_V	VRAM_TYPE_V	VRAM_TYPE_V
VRAM_TYPE_V	VRAM_TYPE_V	VRAM_TYPE_V
VRAM_TYPE_V	VRAM_TYPE_V	VRAM_TYPE_V



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<https://vinafix.com>

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Title		
(RESERVED)		
Size A4	Document Number LS720	Rev -1N
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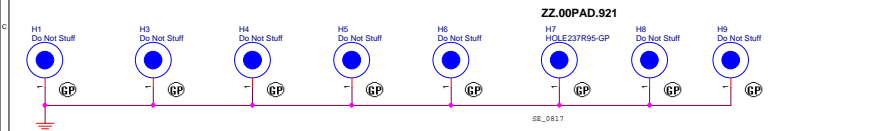
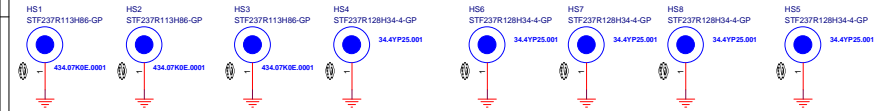
<https://vinafix.com>

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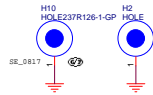
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Title		
(Reserved)		
Size A4	Document Number LS720	Rev -1N
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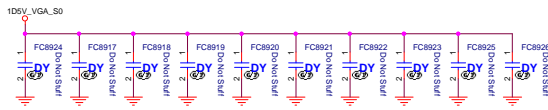
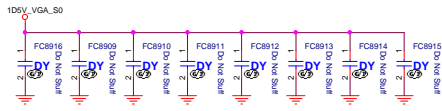
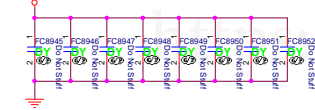
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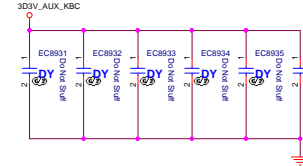
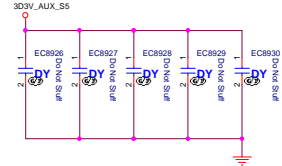
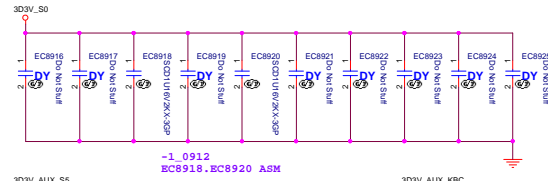
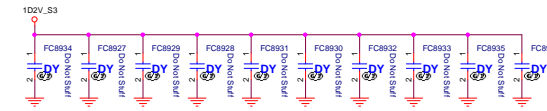
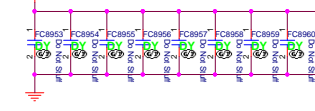
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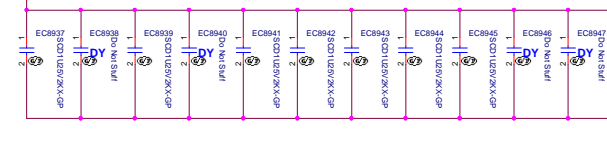
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3D3V\_MSATA1\_S0\_0808



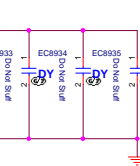
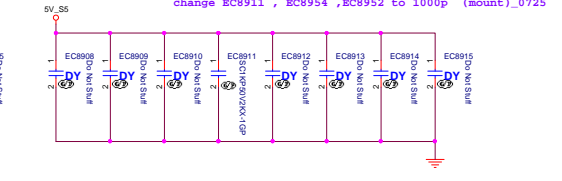
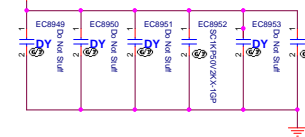
SE\_Add 3D3V\_S0 Dummy 0402 caps X12\_0808



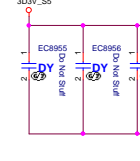
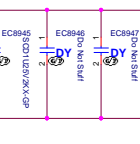
mount EC8942,EC8943,EC8937,EC8941,EC8939\_0725



change EC8911 , EC8954 ,EC8952 to 1000p (mount)\_0725

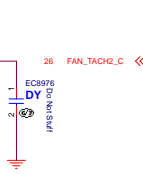
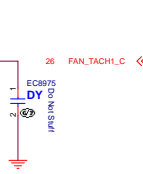
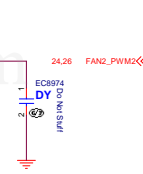
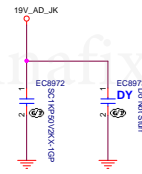
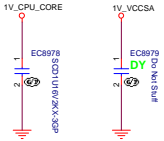


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EC8944.EC8945 ASM

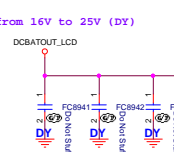
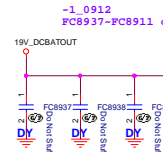


add EC8978 0.1u cap in 1V\_CPU\_CORE  
L10(6293,4311)\_0725

add EC8979 0.1u cap in 1V\_VCCSA  
L1(6746,4244)\_0725\_DY\_MAIL



SD\_Del between power TBTA.VBUS20 and GND  
->EC8969.EC8970.EC8971 (78.10421,2PL)



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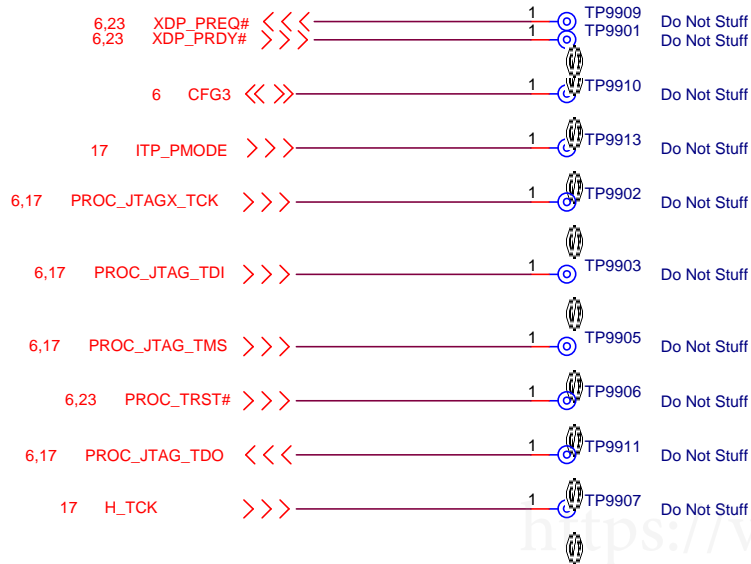
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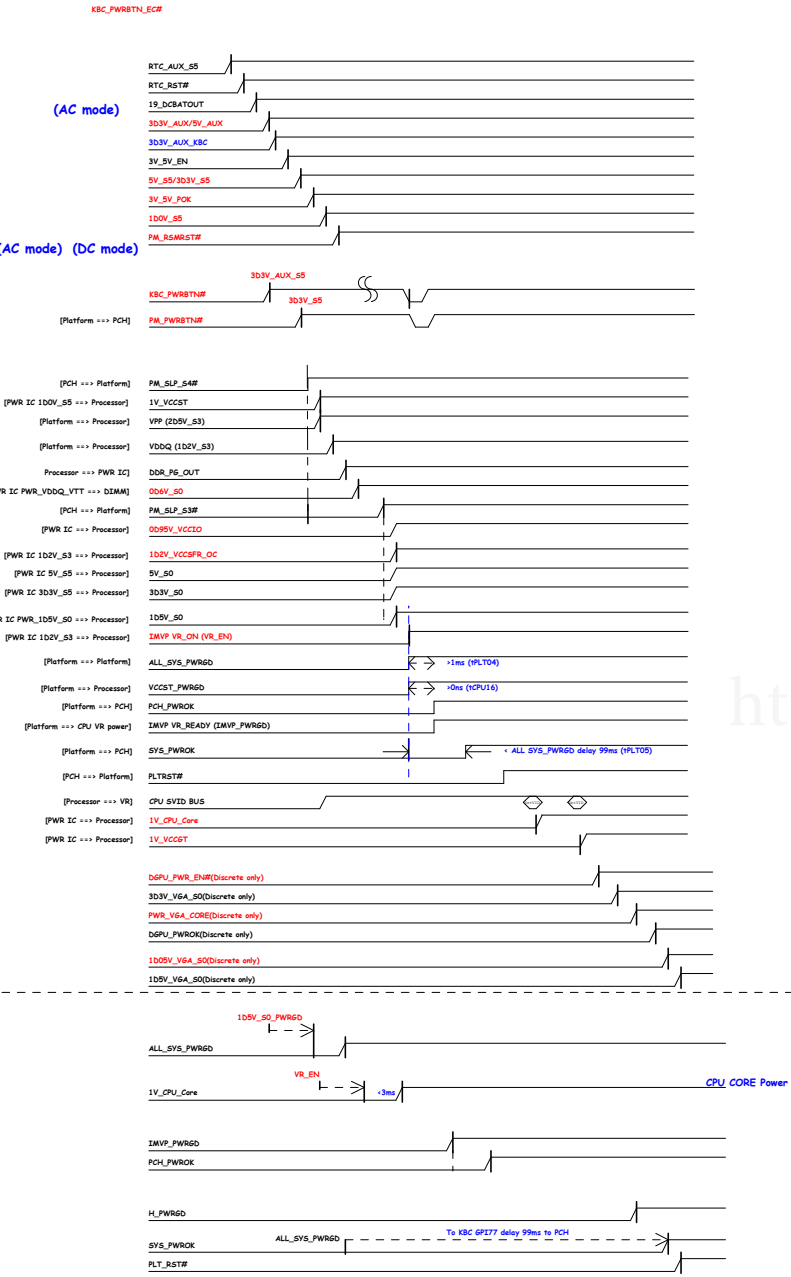
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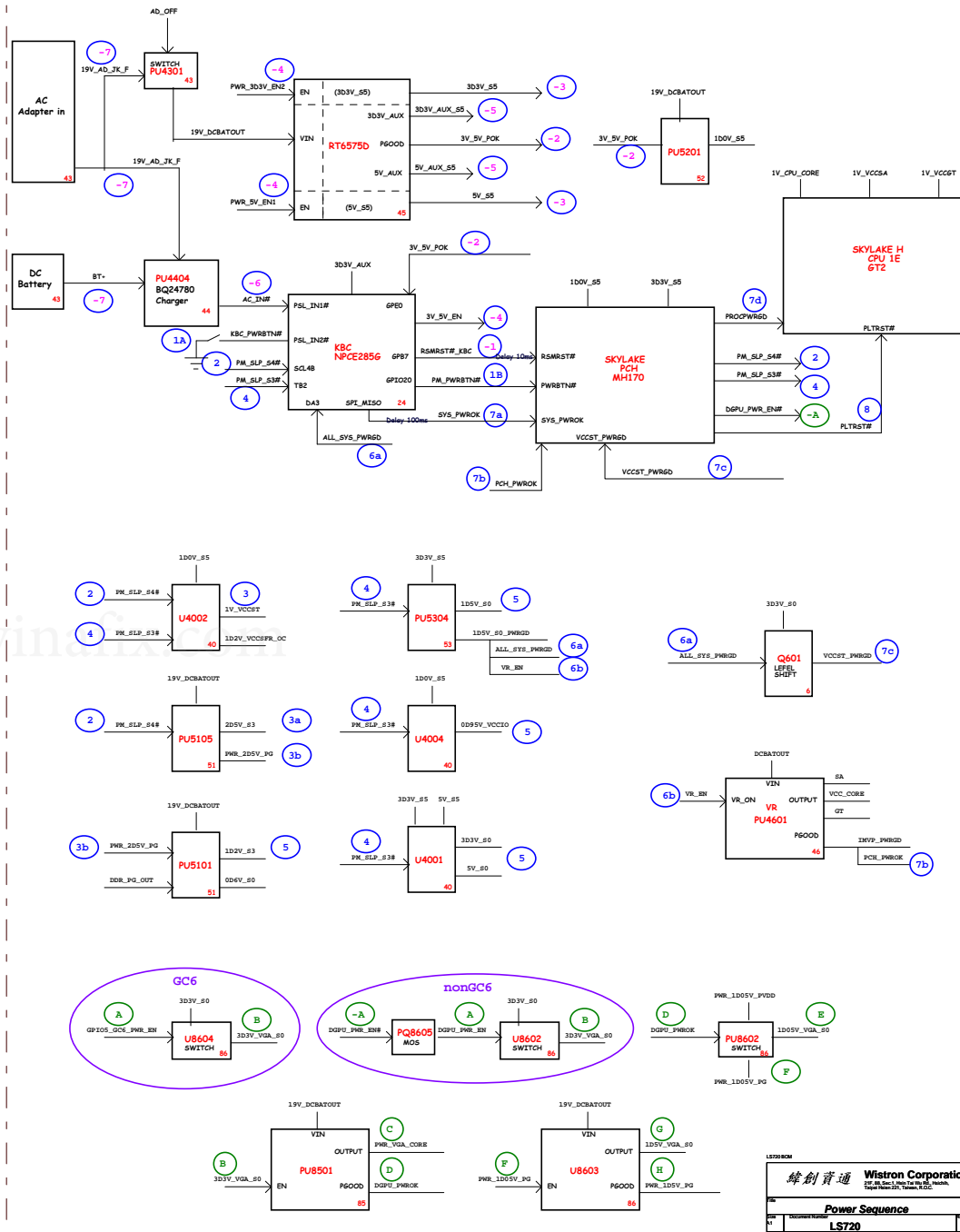
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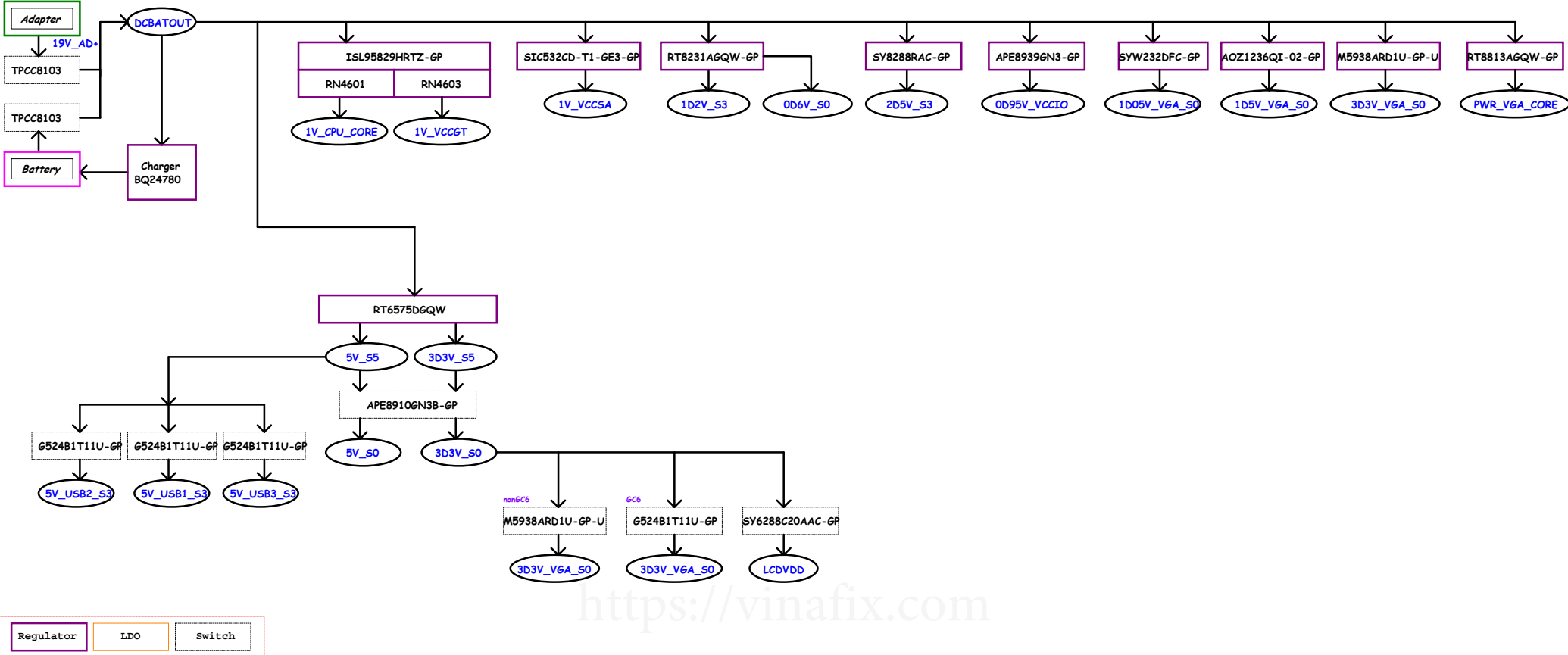
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Intel-Power Up Sequence



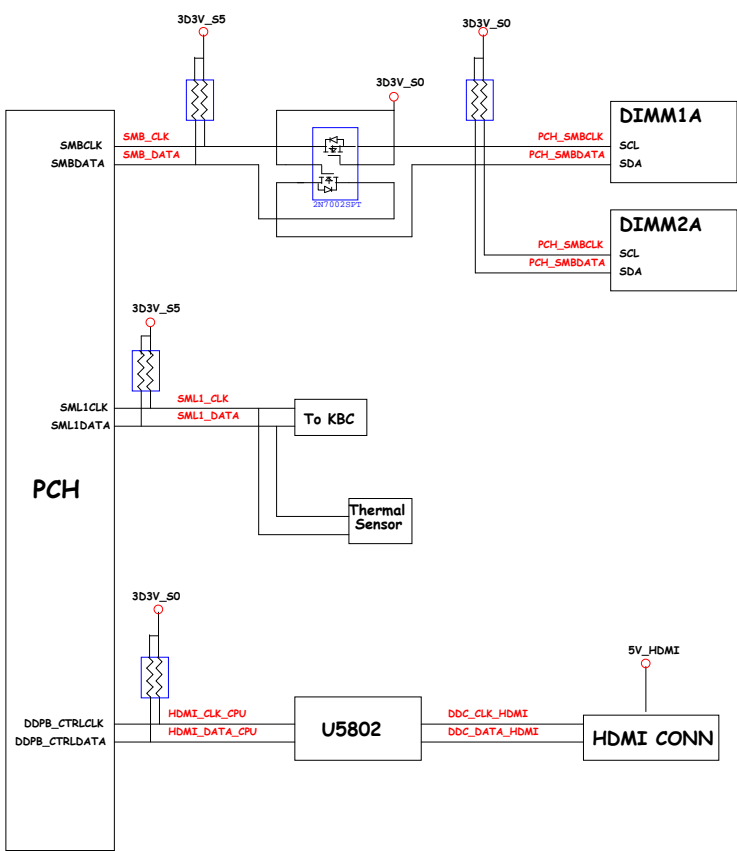
SKYLAKE H POWER UP SEQUENCE DIAGRAM



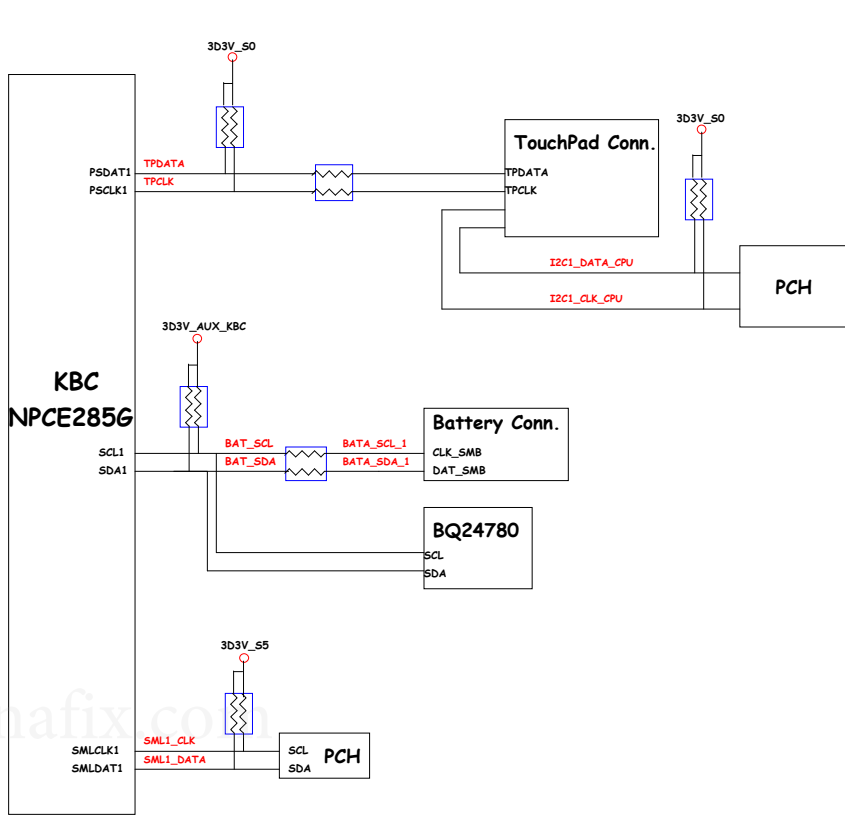


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PCH SMBus Block Diagram

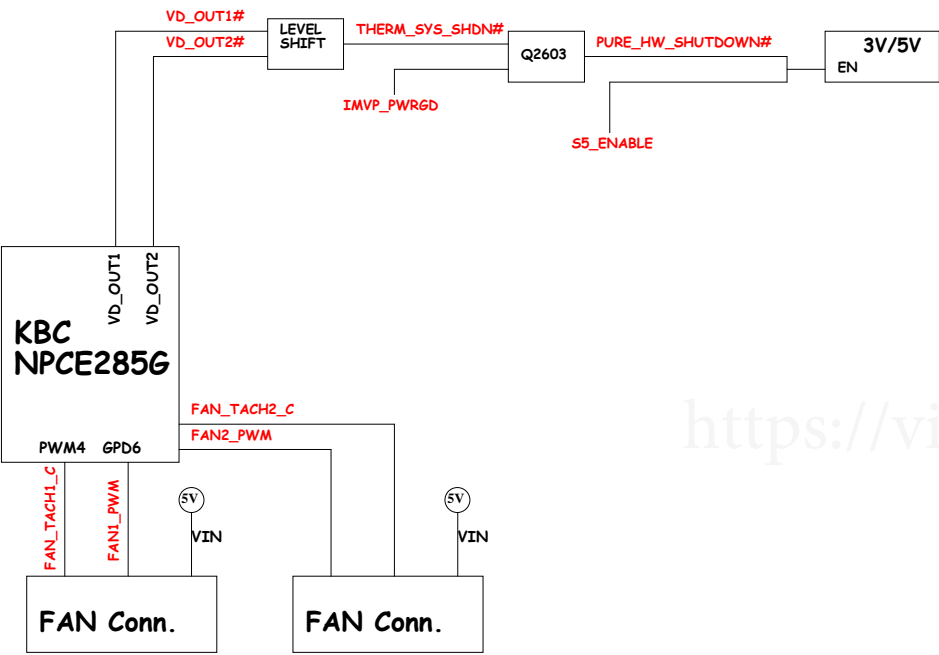


KBC SMBus Block Diagram

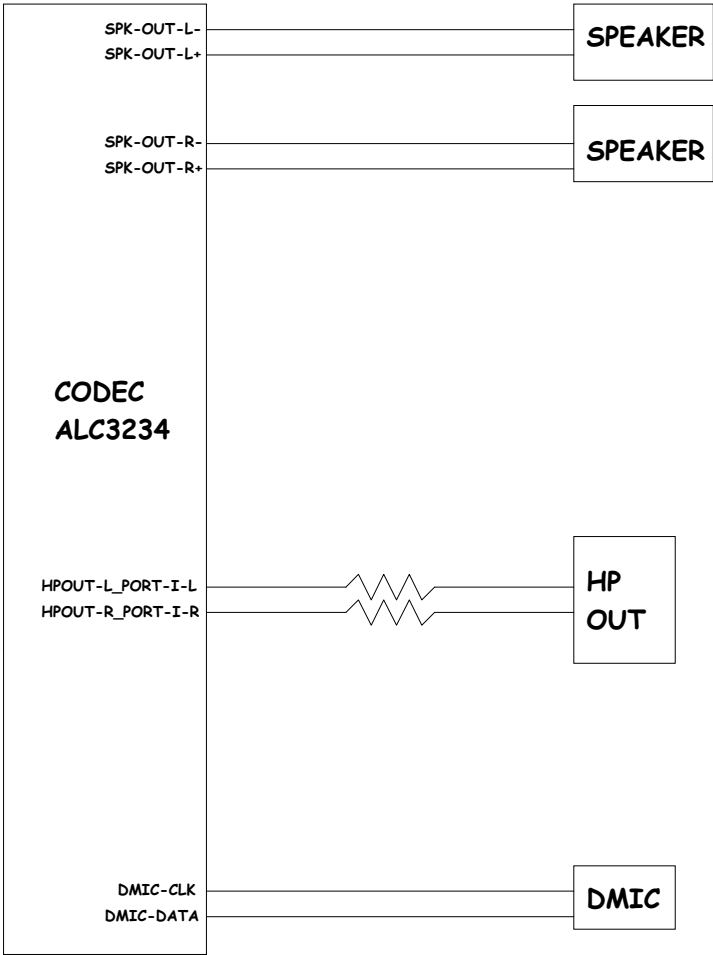




# Thermal Block Diagram



# Audio Block Diagram



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